MCDCM4613

Single-Channel 8A DC/DC Converter

Features

- Low-noise switching power supply
- Input voltage range: 5.0V to 36V
- Adjustable output voltage: 3.3V to 15V
- Output current: Single-channel 8A
- Voltage regulation: ≤1.5%
- Load regulation: ≤1.5%
- Pre-bias startup capability
- Multi-phase parallel current sharing
- External frequency synchronization
- Current-mode control with fast transient response
- PGOOD Function
- Soft-start/output voltage tracking
- Overcurrent, short-circuit, and overtemperature protection
- Package options:
  LGA: 15mm × 15mm × 4.32mm
  BGA: 15mm × 15mm × 4.92mm

Applications

- Radar and communication systems
- Motherboards and CPUs

Description

The MCDCM4613 is a fully integrated single-channel 8A output, wide-input DC/DC converter available in LGA and BGA packages. The module integrates a switching controller, power FETs, inductors, and all supporting components. The input voltage range is 5.0V to 36V, delivering an adjustable output voltage of 3.3V to 15V (set by a single external resistor). Only bulk input and output capacitors are required externally (a combination of ceramic and electrolytic capacitors is recommended).

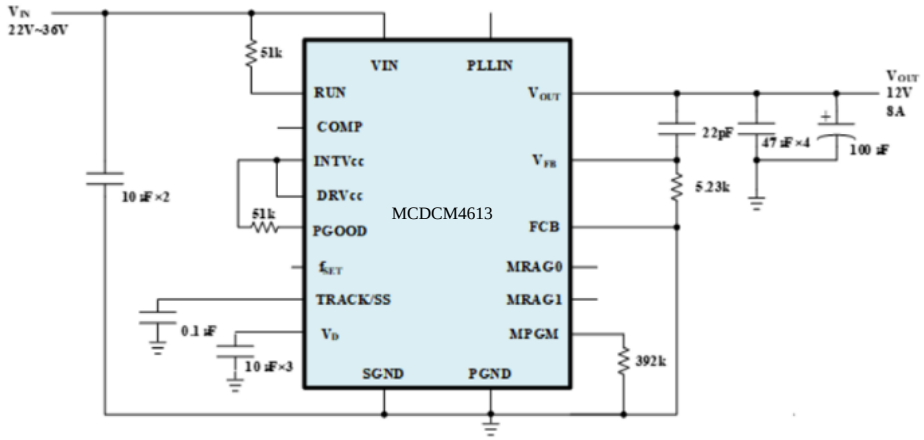
The MCDCM4613 employs DCM startup to prevent reverse current from the output capacitor to the input during startup, eliminating input voltage spikes.

Designed to provide stable power for digital circuits such as communication systems and CPUs, the MCDCM4613 delivers up to 8A continuous output current in standalone operation. When configured in multi-phase parallel mode, it supports 16A (2-phase) or 32A (4-phase) output currents.

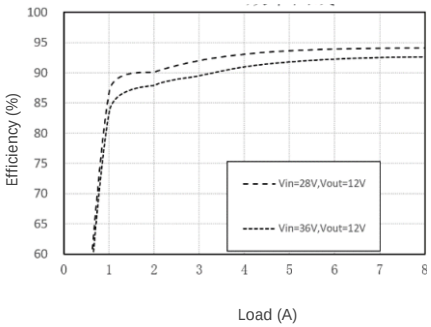
As a surface-mount module, the MCDCM4613 is assembled via reflow soldering onto PCBs, offering compact size, high integration, and lightweight design.

Typical Application

Typical application circuit (single path 8A, 12V)



12V Output Load Efficiency Curve



AbsoluTe Maximum Ratings Note1

V_{IN}, V_D.....-0.3V～36V

V_{OUT}.....-0.3V～16V

RUN.....-0.3V～5.0V

$INTV_{CC}$, DRV_{CC}.....-0.3V ~ 6.0V

PGOOD, TRACK/SS, PLLIN, FCB, MPGM, MARG0, MARG1.....-0.3V～$INTV_{CC}$+0.3V

V_{FB}, COMP.....-0.3V～2.7V

Output current range：

I_{OUT}=0～8A.....Single-channe lindependent operation

I_{OUT}=N×(0～8A)....N represents the number of parallel channels.

Pin soldering resistance temperature.....250°C(30s)

Storage temperature range(T_{stg}).....-55°C～125°C

Recommended Operating Conditions

Input Power Voltage

V_{IN}.....5.0V-36V

Output Voltage Range

V_{OUT}.....3.3-15V

Output Current Range

I_{OUT}....0-8A (single-channel standalone operation)

I_{OUT}.....Nx(0-8A) N:number of parallel channels

Operating Case Temperature (T_C).....-40°C-125°C

Recommended PCB Soldering Temperature Profile:

Standard leaded profile (Peak temperature: 210°C -230°C, Time above liquidus: 30s~90s)

Standard lead-free profile (Peak temperature: 240 °C-245°C, Time above liquidus: 30s~90s).

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Extended operation under absolute maximum conditions may affect device reliability and lifespan.

Thermal Resistance

Model	Package	Dimensions (mm)	Test Board Size (mm)	Junction-to-Ambient θ_{JA}	Junction-to-Substrate $\theta_{JCbottom}$	Junction-to-Top θ_{JCtop}
MCDCM4613L	LGA	15×15×4.32	≧130×130 (4-layer)	9°C/W	2.2°C/W	16°C/W
MCDCM4613B	BGA	15×15×4.92	≧130×130 (4-layer)	9°C/W	2.4°C/W	16°C/W

Test Conditions: Mount the product onto a test board measuring 130mm × 130mm × 1.6mm, constructed as a 4-layer PCB with 1ozcopper pours on both outer and inner layers. Since thermal resistance parameters are closely tied to the actual application environment, measured results may vary under different conditions. These values should be considered for reference purposes only.

Odering Information

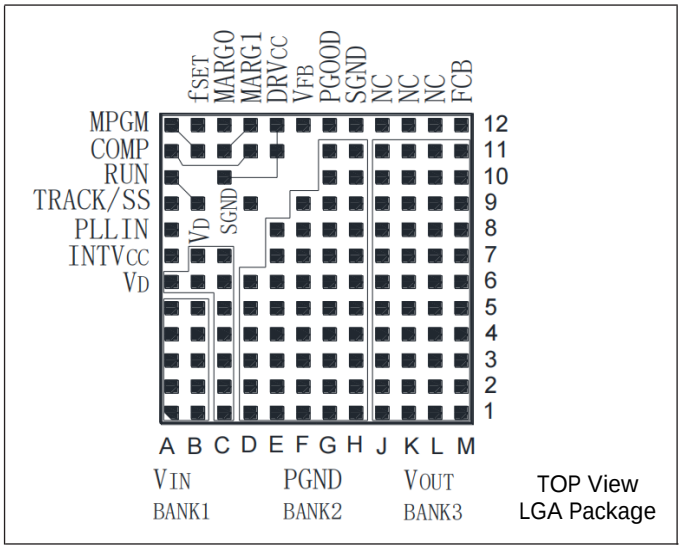
Device Specification	Terminal Material	Package Type	Moisture Sensitivity Level	Temperature Range (T_j)	Quality Grade
MCDCM4613L	Ni-Pd-Au	133-LGA	3	-40°C-125°C	Industrial Grade
MCDCM4613B	Sn63Pb37	133-BGA	3	-40°C-125°C	Industrial Grade

Electrical Characteristics • indicates -55℃ ≤ Tc ≤ 125℃. Unless otherwise specified, all test conditions are TA = 25℃.

Symbol	Parameter	Test Condition (Note2)		Limits			Unit
				Min	Typ	Max	
V_{IN}	Input Voltage	—	•	5	—	36	V
V_{OUT}	Output Voltage	C_{IN}=10μF×2/ceramics, C_D=10μF×3/ceramics, C_{OUT}=47μF×4/ceramics, FCB=0V, V_{IN}=24V、36V, V_{OUT}=12V	•	11.76	12.00	12.24	V
Input Characteristics							
$V_{IN(UVLO)}$	Undervoltage Lockout	I_{OUT} = 0A		—	3.2	4.8	V
$I_{Q(SVIN)}$	Quiescent Current	V_{IN}=36V, V_{OUT}=12V, I_{OUT} = 0A		—	80	100	mA
		V_{IN}=24V, V_{OUT}=12V, I_{OUT} = 0A		—	70	100	mA
		Shutdown, RUN=0, V_{IN}=36V		—	300	600	μA
$I_{S(VIN)}$	Input Supply Current	V_{IN}=24V, V_{OUT}=12V, I_{OUT} = 8A		—	4.26	—	A
		V_{IN}=36V, V_{OUT}=12V, I_{OUT} = 8A		—	2.9	—	
V_{INTVCC}	Internal Vcc Voltage	V_{IN}=36V, RUN＞2V, I_{OUT}=0A		4.7	5.0	5.3	V
Output Characteristics							
$I_{OUT(DC)}$	Output Current	V_{IN}=24V, V_{OUT}=12V		0	—	8	A
S_V	Line Regulation	V_{OUT}=12V, I_{OUT}=0A, V_{IN}=24V~36V, FCB=0V	•	—	0.5	1.5	%
S_I	Load Regulation	V_{IN}=24V, V_{OUT}=12V, I_{OUT}=0A~8A, Room temperature, Low temperature	•	—	—	1.5	%
		V_{IN}=24V, V_{OUT}=12V, I_{OUT}=0A~4A, high temp.	•	—	—	1.5	%
V_{PP}	Output Ripple Voltage	I_{OUT}=8A, C_{OUT}=47μF×4/ceramics+100μF×1/tantalum V_{in}=24V, V_{OUT}=12V, Room temperature, Low temperature	•	—	30	50	mV
		I_{OUT}=4A, C_{OUT}=47μF×4/ceramics+100μF×1/tantalum V_{in}=24V, V_{OUT}=12V, High temperature		—	30	50	mV
f_S	Switching Frequency	V_{IN}=24V, V_{OUT}=12V, I_{OUT}=0A, fset Floating		550	700	850	kHz
$\triangle V_{OUT(START)}$	Startup Overshoot	C_{OUT}=47μF×4/ceramics, V_{IN}=24V V_{OUT}=12V, I_{OUT}=0A, C_{SS}=0.1uF		—	—	20	mV
t_{START}	Startup Time	C_{OUT}=47μF×4/ceramics+100μF×1/tantalum, No-Load, C_{SS}=0.01μF, V_{IN}=24V, V_{OUT}=12V		—	—	0.5	ms
$\triangle V_{OUTLS}$	Dynamic Load Overshoot Voltage	Load: 0A~4A~0A, V_{IN}=24V, V_{OUT}=12V C_{OUT}=47μF×4/ceramics+100μF×1/tantalum		—	260	400	mV
t_{SETTLE}	Dynamic Load Recovery Time	Load: 0A~4A~0A, V_{IN}=24V, V_{OUT}=12V C_{OUT}=47μF×4/ceramics+100μF×1/tantalum		—	150	300	μs
I_{OUTPK}	Output Current Limit Threshold	V_{IN}=24V, V_{OUT}=12V		12	16	24	A
Control section							
V_{FB}	Error Amplifier Input Voltage Accuracy	V_{IN}=24V, V_{OUT}=12V, I_{OUT}=0A		0.59	0.60	0.61	V
V_{RUN}	RUN Pin Turn-On/ Off Threshold	—	•	1.0	1.5	1.9	V

Note2:The electrical characteristic tests are conducted under laboratory conditions, where the module is soldered to the evaluation board 2 for testing.

PIN Configuration



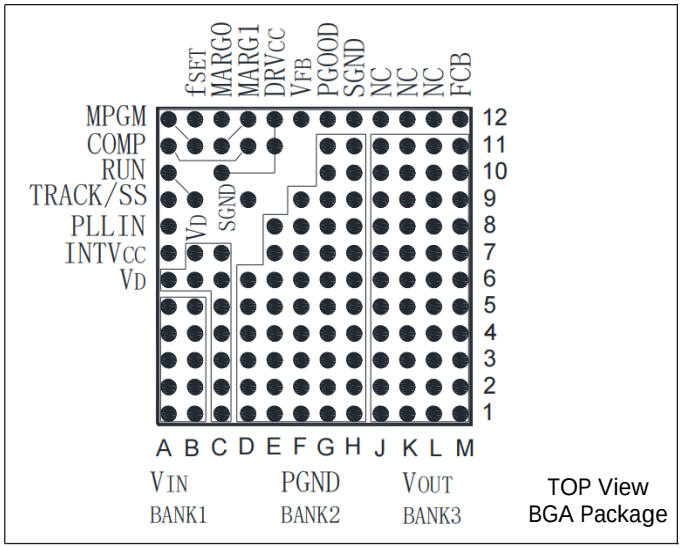


Figure 1. Pin defines the top view

PIN	Definition	Pin Description
A1-A5, B1-B5	V_{IN}	Power input pin. Connect filter capacitors directly between input and ground.
D1-D6, E1-E8, F1-F9, G1-G11, H1-H11	PGND	Power ground for input and output circuits.
J1-J11, K1-K11, L1-L11, M1-M11	V_{OUT}	Power output pin. Connect filter capacitors directly between output and ground.
A6, B6-B7, C1-C7	V_D	Top FET drain pin. Connect high-frequency ceramic decoupling capacitors between VP and PGND to handle RMS current and reduce input ripple.
C10, E11-E12	DRV_{CC}	External power input. Typically connected to $INTV_{CC}$ to supply internal drivers.
A7	$INTV_{CC}$	Internal 5V reference output.
A8	PLLIN	External synchronization clock input.
M12	FCB	Forced continuous input. Connect to SGND to force continuous conduction mode at light loads. Do not connect high or leave floating (currently unsupported).
A9	MPGM	Output voltage tracking and soft-start input. Controls output rise time.
A12, B11	PGOOD3	Programmable margining input. Fixed ±10% margining adjustment range.
B12	PGOOD1	Frequency setting. Connect resistor to ground to increase frequency; to V_{IN} to decrease frequency.
F12	PGOOD2	Inverting input of error amplifier. Internally connected to VOUT via 100kΩ precision resistor. Set output voltage with external resistor between VFB and SGND. For parallel operation: Connect all VFB pins together.
C12	PGOOD4	LSB logic input for margining. Determines high/low/no margining state with MARG1.
C11, D12	CLKOUT	MSB logic input for margining. Determines high/low/no margining state with MARGO.

PIN	Definition	Pin Description
D9, H12	SGND	Signal ground pin.
A11, D11	COMP	Current control threshold & error amplifier compensation point. For parallel operation: Connect all COMP pins for current sharing.
G12	PGOOD	Output status indicator. Open-drain output pulls low when output voltage exceeds ±10% of nominal value.
A10, B9	RUN	Enable control. Module turns on >1.9V; turns off <1V.
J12, K12, L12	MTP	Do not connect. Leave floating.

Product Principle Block Diagram

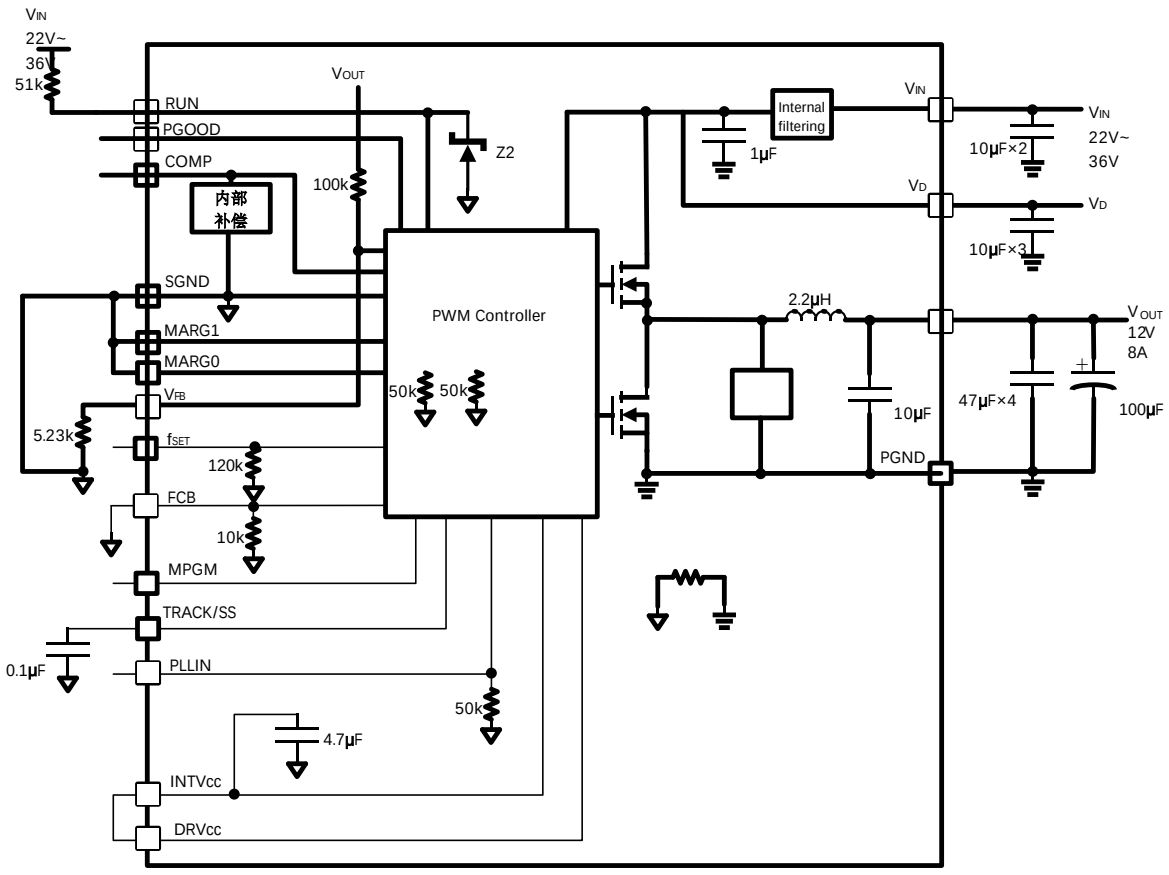


Figure 2. Block diagram of the principle of MCDCM4613

Typical Performance Characteristics

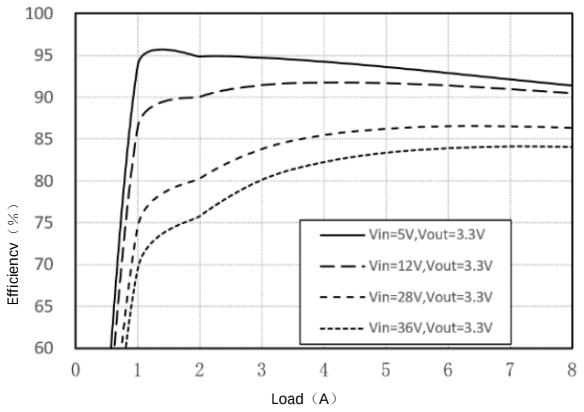


Figure 3. 3.3V output-load-efficiency curve

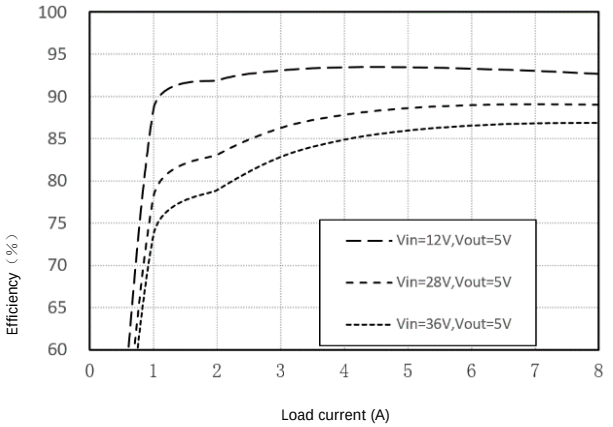


Figure 4. 5V output-load-efficiency curve

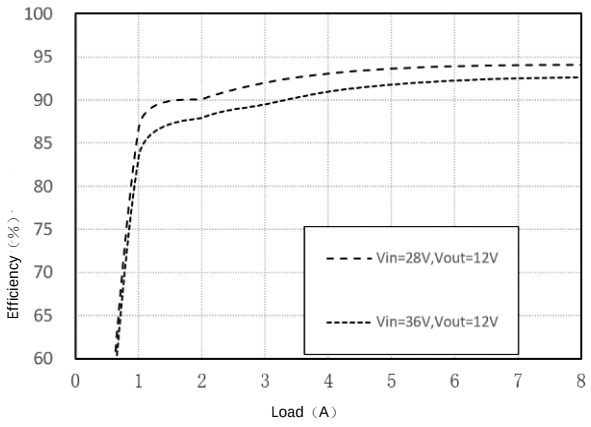


Figure 5. 12V output-load-efficiency curve

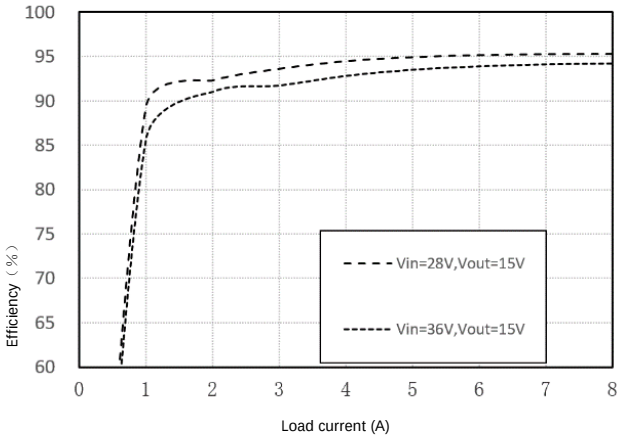
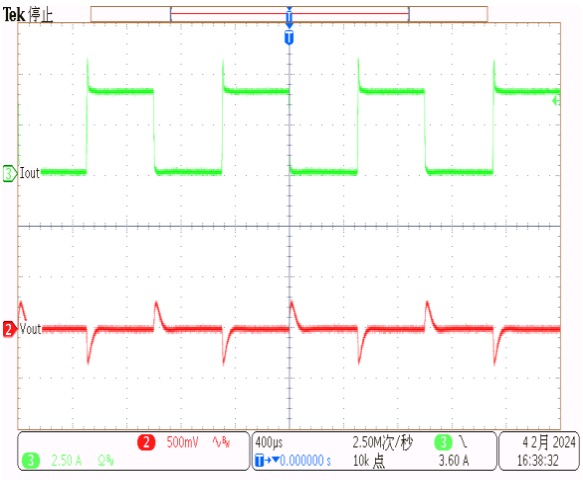


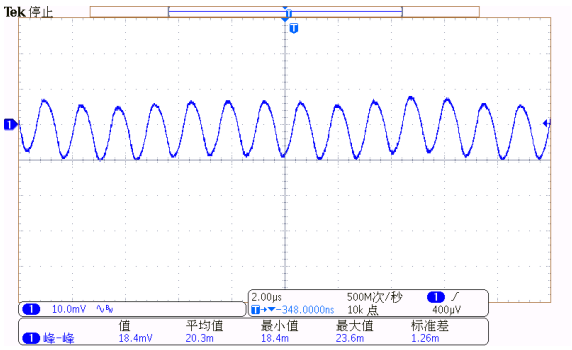
Figure 6. 15V output-load-efficiency curve



V_{IN} =28V； V_{OUT} =12V； I_{OUT} =0~4A~0A；

f=5kHz， C_{OUT} =47μF(ceramic)×4+2×100uF (Tantalum)

Figure 7. Load-dynamic curve



V_{IN} =28V； V_{OUT} =12V； I_{OUT} =8A； BW=20MHz,

C_{OUT} =47μF(ceramic)×4+2×100uF (Tantalum)

Figure 8. Output Ripple Waveform at Full Load

Typical Performance Characteristics

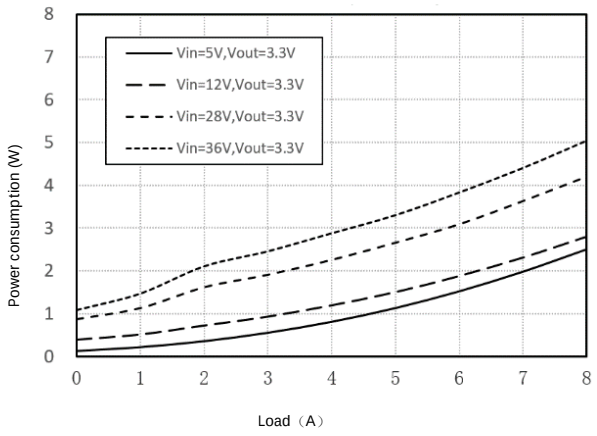


Figure 9. Power consumption curve at 3.3V output voltage (25℃)

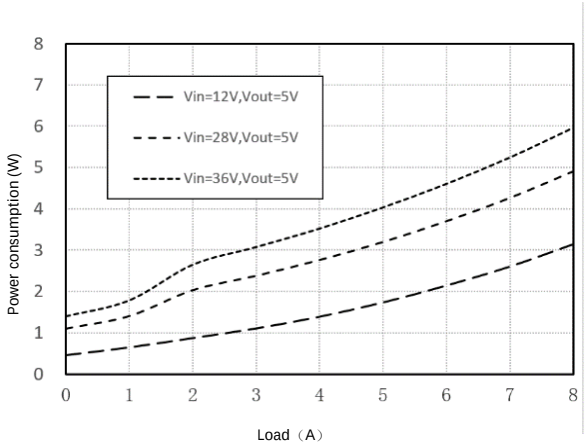


Figure 10. Power consumption curve at 5V output voltage (25℃)

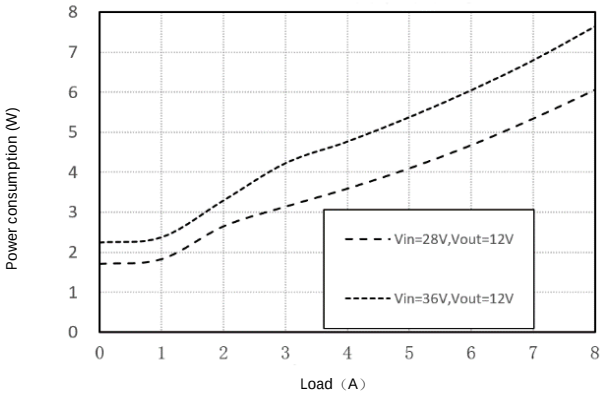


Figure 11. Power consumption curve at 12V output voltage (at 25℃)

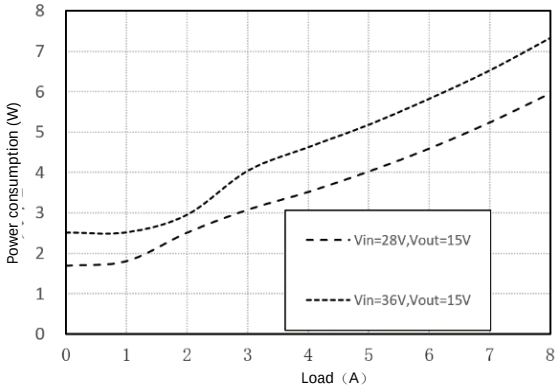


Figure 12 Power consumption curve at 15V output voltage (25℃)

Application Instructions

Output voltage

The PWM controller's reference voltage is 0.6V. As shown in Figure 2, a 100kΩ internal feedback resistor connects between the V_{OUT} pin and FB pin. Adding an external resistor R_{FB} between the FB pin and GND sets the output voltage:

$$V_{OUT}=0.6V\times\frac{100k\Omega+R_{FB}}{R_{FB}}$$

Table 1: Output Voltage vs. R_{FB} Resistance Values

V_{OUT}(V)	3.3	5	8	10	12	15
R_{FB} (kΩ)	22.1	13.7	8.06	6.34	5.23	4.12

Input decoupling capacitor

The MCDCM4613 must be connected to a low-AC-impedance DC source. A 22μF ceramic input capacitor is recommended for RMS ripple current decoupling.

If extended input traces, parasitic inductance, or insufficient capacitance exist, add one high-capacitance input capacitor (e.g., tantalum type).

Ignoring inductor current ripple, estimate the input capacitor RMS current using:

$$I_{CIN(RMS)}=\frac{I_{OUT(MAX)}}{\eta\ \%}\times\sqrt{D\times(1-D)}$$

η% in the formula represents the estimated efficiency of the power module.

Output decoupling capacitor

Output capacitors must utilize low-ESR types to achieve low output voltage ripple and superior transient response. To ensure filtering performance and stability across three-temperature environments, the total output capacitance should not be less than 200μF. System designers may configure output filtering capacitors based on actual application requirements. For enhanced high -frequency noise suppression, add parallel capacitors (e.g., 1μF, 0.1μF, 1000pF).

Output filter capacitors must be fully integrated into the power loop (refer to PCB layout diagram).

Working frequency

The operating frequency of the MCDCM4613 has been optimized during design to achieve high efficiency while maintaining compact package size and low output ripple voltage. The switching frequency is programmed via an external resistor connected to the fset pin.

Table 2. Phase Difference Between Stabilizer Channels

V_{OUT}	FSET pin ground resistance R_{fset}	Work frequency
3.3V	93kΩ	450kHz
5V	133kΩ	550kHz
8V	NC	490kHz
10V	NC	620kHz
12V	NC	700kHz
15V	f_{SET} connected to V_{IN} via 5.1MΩ resistor	680kHz

The power module incorporates a phase-locked loop consisting of an internal voltage-controlled oscillator and phase detector. This enables synchronization of all internal switching MOSFET turn-on events to the rising edge of an external clock. The external clock frequency must be within ±30% of the 1MHz set frequency. A pulse detection circuit activates the PLL upon detecting a clock signal at the CLKIN pin. The clock pulse width must be at least 400ns.

Clock HIGH level must exceed 2.5V, while clock LOW level must remain below 0.3V

Parallel operation

The MCDCM4613 allows parallel operation of modules to deliver higher output current. N-phase (8A per phase) parallel configuration is applicable for:

$$V_{OUT}=0.6V\times(1+\frac{100k\Omega/N}{R_{FB}})$$

The MCDCM4613 employs current-mode control, enabling exceptional current-sharing characteristics in parallel operation to achieve thermal balance. For parallel configurations:

RUN, TRACK/SS, V_{FB}, and COMP pins must be connected together across all modules.

Soft start and output voltage tracking

The TRACK/SS pin enables soft-start functionality and output voltage tracking during startup. Connecting a capacitor between the TRACK/SS pin and ground sets the output voltage establishment time. An internal 1.5 μA current source charges the external soft-start capacitor to approximately the internal reference voltage of 0.6V. The total soft-start time can be calculated using the following formula:

$$t_{SS} = \frac{C_{SS}}{1.5\mu A} \times 0.6V$$

In the formula, CSS represents the capacitor on the TRACK/SS pin.

By modifying the connection method of TRACK/SS, the output can also be made to track the rise or fall of another voltage regulator. Figures 13 and 14 show example waveforms and a schematic diagram for coincident tracking.

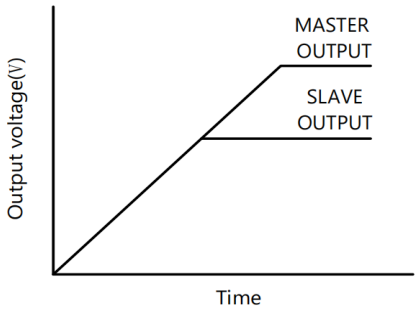


Figure 13. Overlapping Tracking Schematic Diagram

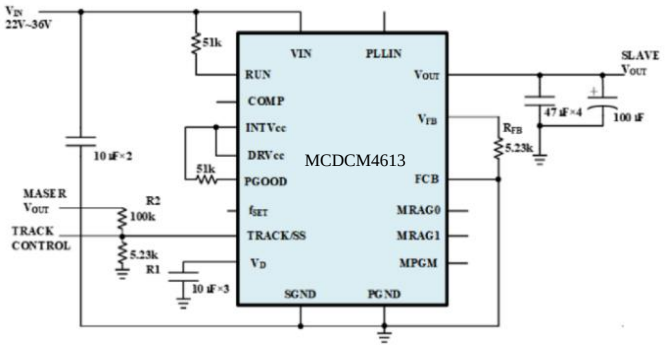


Figure 14. Output Tracking Circuit Diagram

The output slew rate (MR) of the master regulator and the output slew rate (SR) of the slave regulator, in units of V/s, are determined by the following equation:

$$\frac{MR}{SR} \cdot 100k = R2$$

When operating in coincident tracking, MR = SR and R2 = 100 kΩ, R1 can be derived from the following equation:

$$R1 = \frac{0.6V}{\frac{V_{FB}}{100k} + \frac{V_{FB}}{R_{FB}} - \frac{V_{TRACK}}{R_2}}$$

VFB denotes the feedback reference voltage, and VTRACK = 0.6 V. During coincident tracking, R2 = 100 kΩ. When VFB = VTRACK occurs, R1 = RFB = 5. 23 kΩ, as illustrated in Figure 14.

PGOOD function

The PGOOD pin is an open-drain output that indicates whether the output voltage is within regulation. This pin monitors whether the output voltage stays within ±10% of its set value.

Since the PGOOD pin cannot actively drive a high level, an external pull-up resistor is required during use. It is typically recommended to pull this pin up to its own channel's $INTV_{CC}$ pin. The pull-up resistor value can be configured between 4.7 kΩ and 100 kΩ.

Stability compensation

The internal compensation loop of the MCDCM4613 module is specifically designed and optimized for applications utilizing only low-ESR ceramic output capacitors.

In scenarios requiring bulk output capacitors to reduce output ripple and dynamic transient spikes, an additional 22 pF capacitor (CFF) must be added between the VOUT and VFB pins to improve phase margin.

Enable function

The RUN pin serves as a run enable control for turning on the MCDCM4613 switching DC/DC converter. When pulled low, this pin places the MCDCM4613 in shutdown mode.

With a typical threshold voltage of 1.5V, the regulator turns on when the RUN pin voltage exceeds 1.5V.

Recommended PCB Layout

1.Pad Design

The recommended LGA pad size is 0.63 mm × 0.63 mm, while the recommended BGA pad diameter is 0.63 mm.

It is recommended that the open solder mask windows for large-area copper-coated power pins (e.g., V_{IN}, GND, V_{OUT}, etc.) be adjusted and redesigned. Otherwise, the PCB manufacturing company may apply the default solder mask opening width of approximately 0.1 mm as defined by standard software. This could result in actual solder pads being slightly larger than intended, potentially causing discrepancies between the sizes of the solder pads and independent pins. Inconsistent solder mask windows may lead to the module experiencing solder tension-induced stress in the vertical direction perpendicular to the PCB during reflow soldering, which can cause compression or stretching of solder on other independent pads.

2. PCB Layout

To optimize the electrical and thermal performance of the PCB layout, the following considerations should be implemented:

a. Use large PCB copper areas for high-current paths (e.g., V_{IN}, GND, V_{OUT}) to minimize conduction losses and thermal stress;

b. Place high-frequency ceramic capacitors near the V_{IN}, GND, and V_{OUT} pins to suppress high-frequency noise;

c. Implement a dedicated power ground plane beneath the module;

d. Use multiple vias to connect the top layer with other power layers, minimizing via conduction losses and reducing thermal stress;

e. Avoid placing vias directly on pads unless via-in-pad with filled vias is implemented;

f. For parallel modules, connect the COMP, V_{FB}, RUN, and TRACK/SS pins together. Use an internal layer to interconnect these pins.

Figure 15 provides a recommended PCB layout reference.

3. Recommended Solder Pad

For the MCDCM4613B product, the typical BGA solder ball diameter is 0.76 mm. The pad size for the MCDCM4613L variant is 0.65 mm × 0.65 mm. Users are advised to design BGA footprint libraries according to the dimensions specified in Table 3.

Table 3. Recommended Solder Pad Dimensions for MCDCM4613

Product Model	BGA Ball Diameter (mm)	Recommended Solder Mask Opening (mm)
MCDCM4613B	Φ0.76	Φ0.63
MCDCM4613L	N/A	0.63 × 0.63

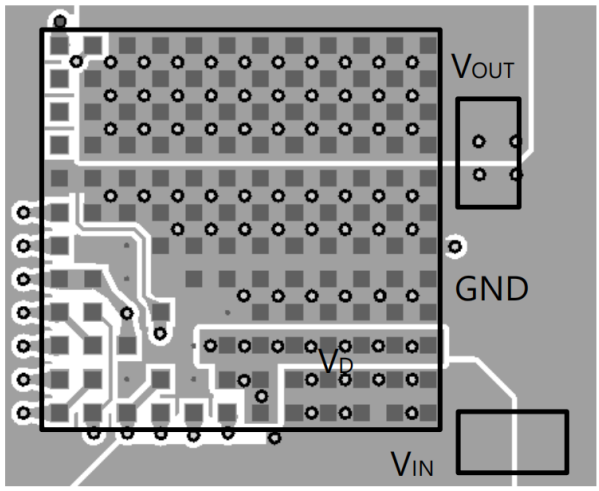


Figure 15. Recommended PCB Layout for MCDCM4613
(The VD capacitor may be placed on the back side of the PCB)

Typical application diagram(Note3)

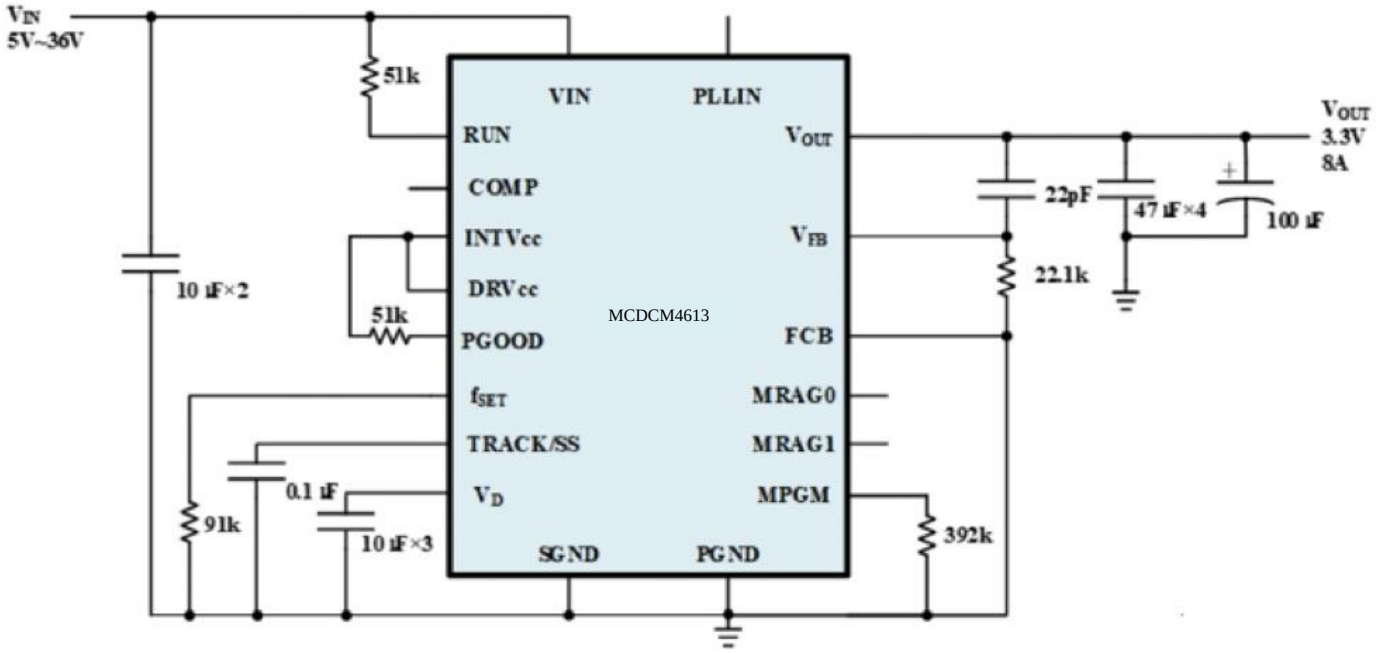


Figure 16. Single-output 3.3V, Load 8A

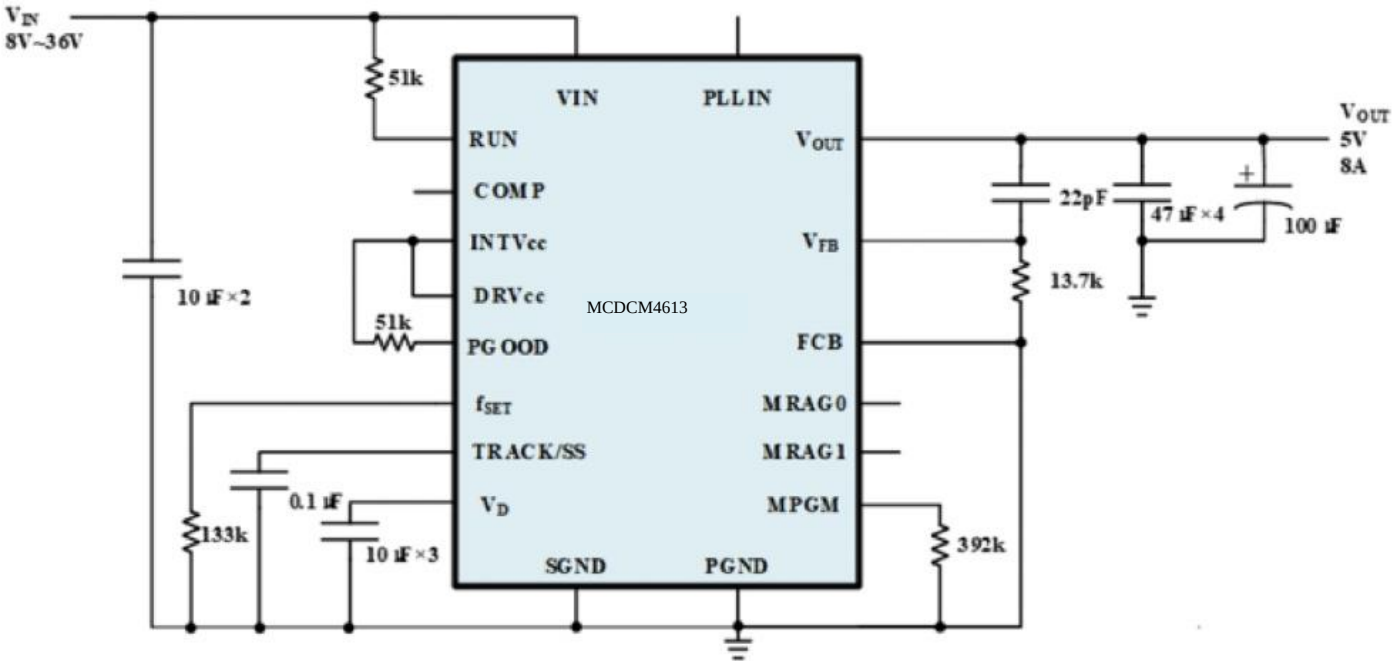


Figure 17. Single-output 5 V, Load 8A

Typical application diagram

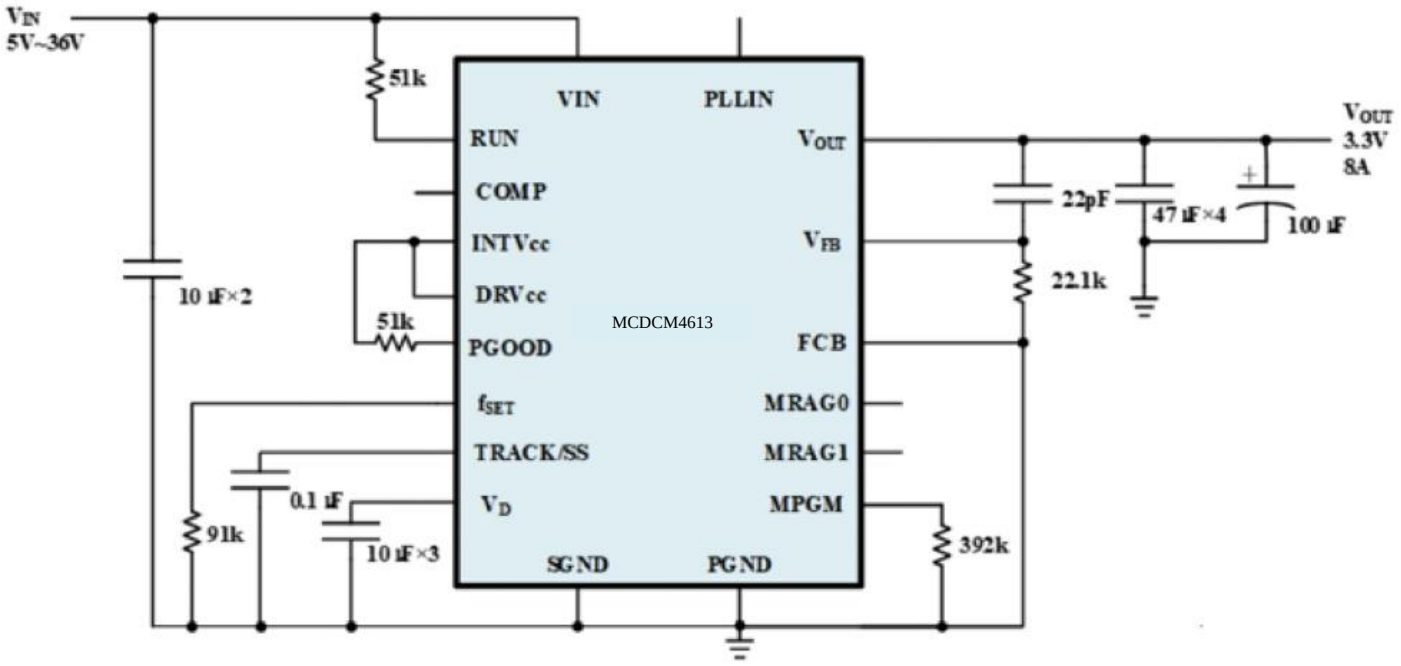


Figure 18. Single-output 12 V, Load 8A

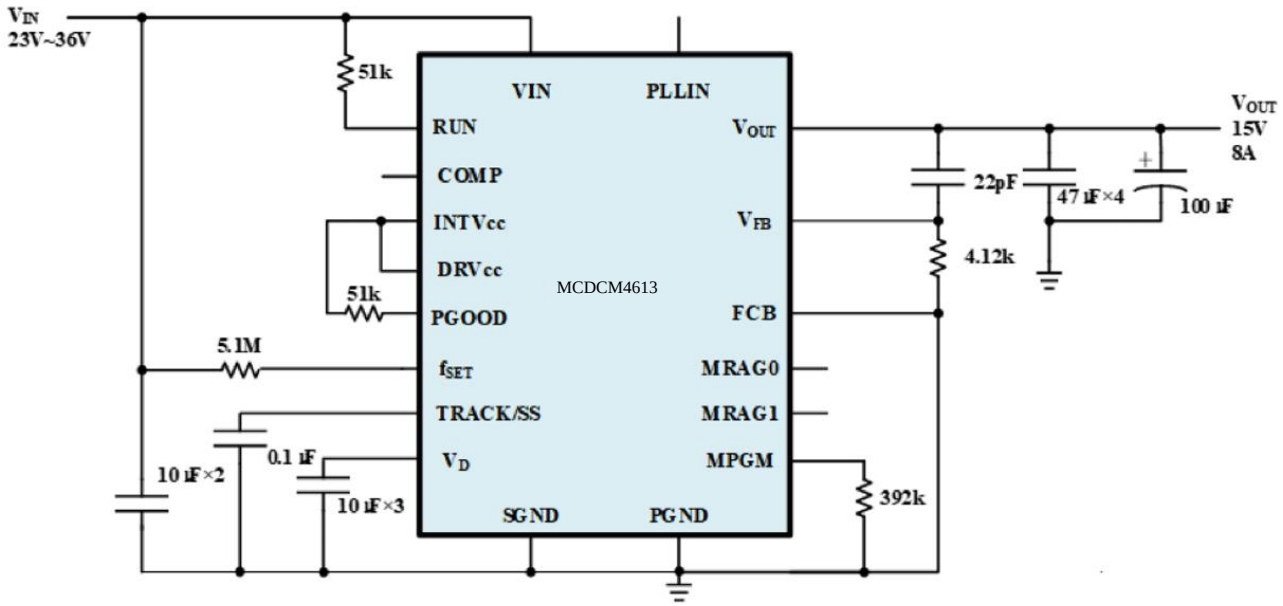


Figure 19. Single-output 15 V, Load 8A

Typical application diagram

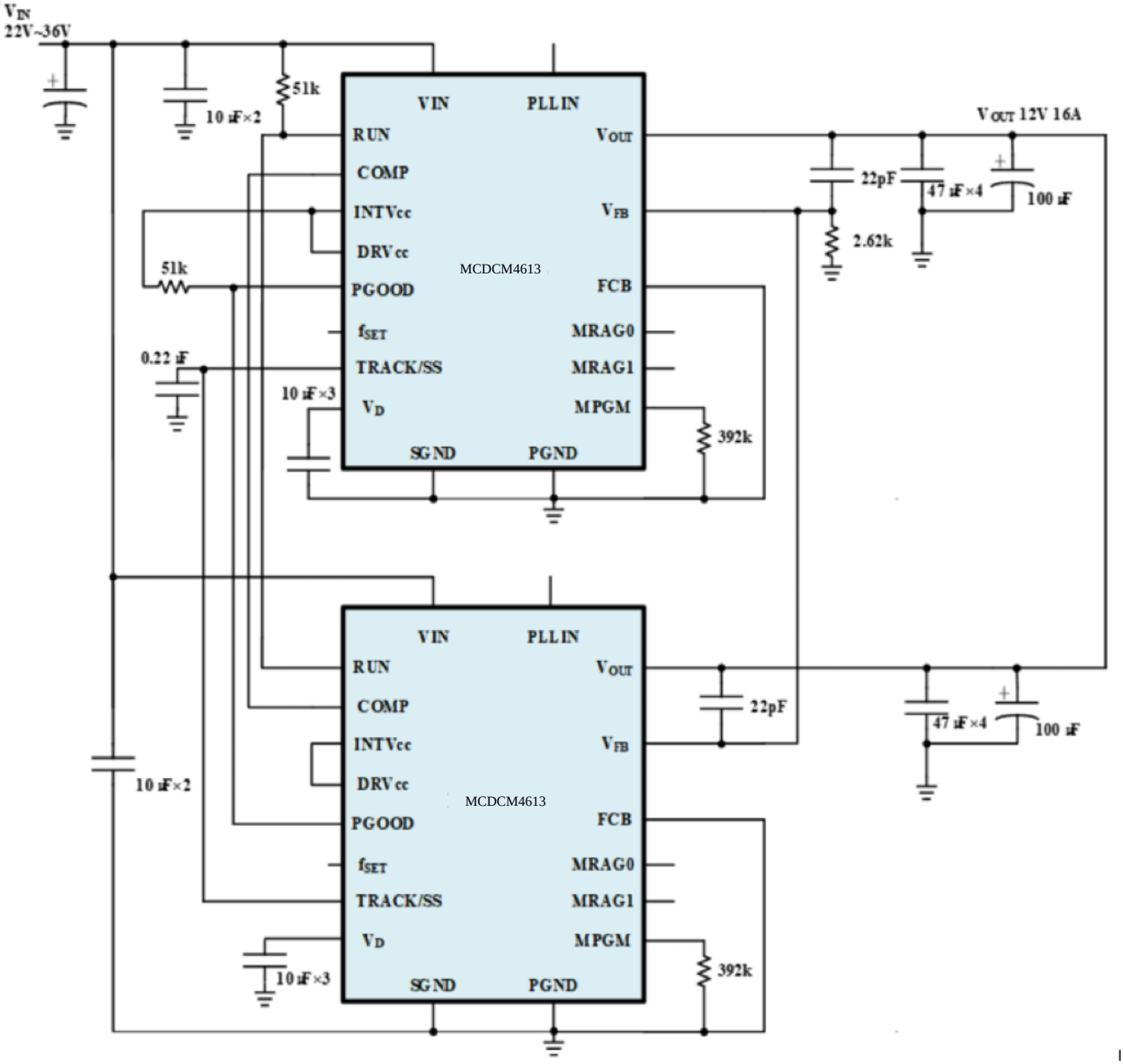


Figure 20. Two-phase parallel output 12V, load 16A
(Connecting PLLIN together can reduce output ripple)

Typical application diagram

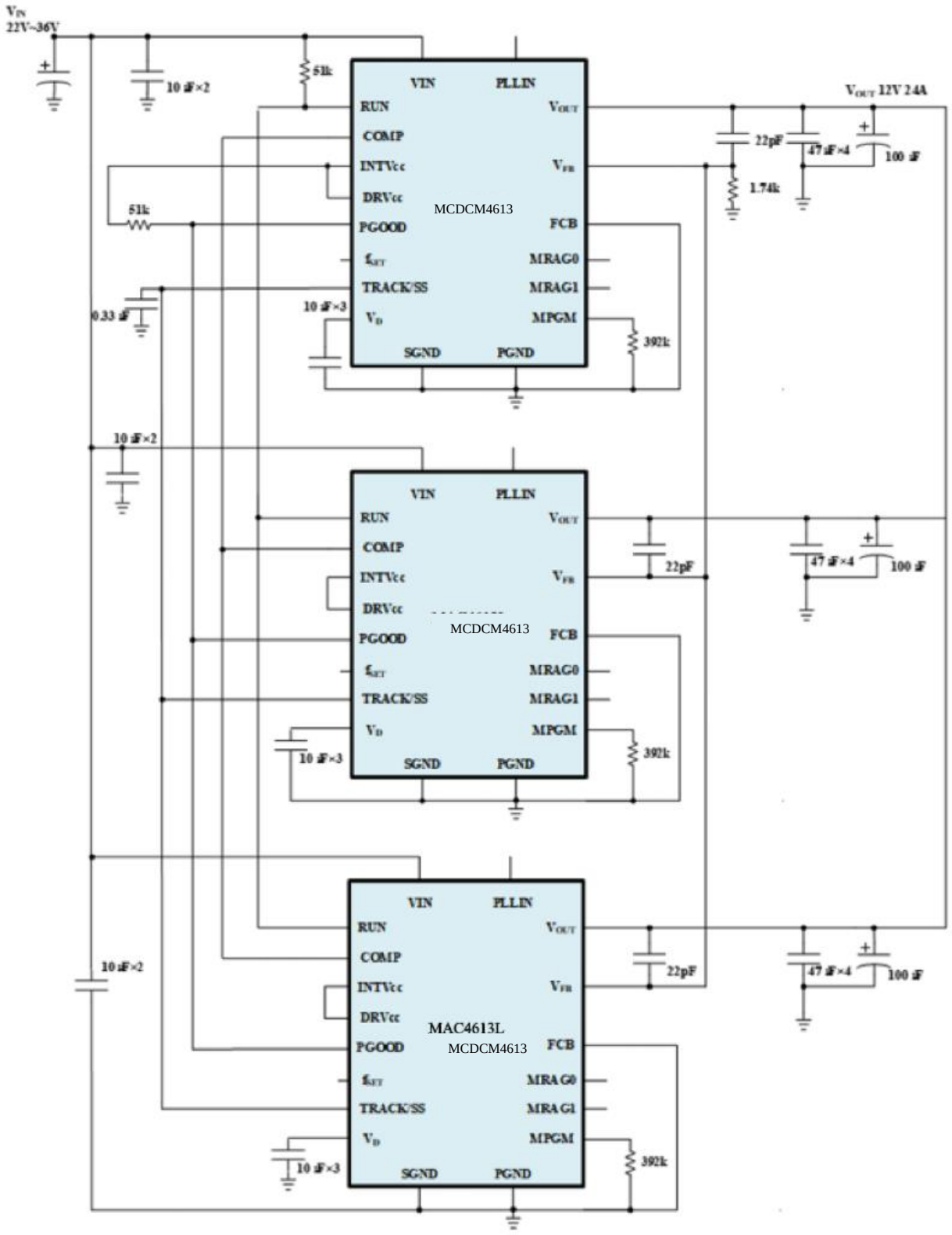


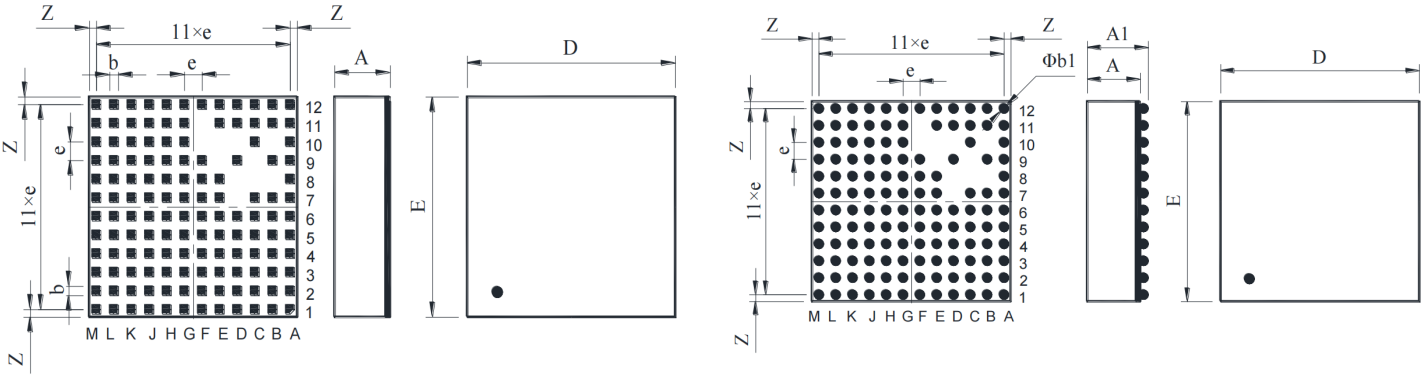
Figure 21 Three-phase parallel output 12V, load 24A
(Connecting PLLIN together can reduce output ripple)

Note 3: The typical application circuit, including the one presented on page 1, is designed based on a configuration that maximizes the module's optimal performance and is applicable to most practical scenarios. When implementing this circuit in practice, users may make appropriate adjustments according to factors such as the board space dimensions and output noise requirements. However, it is not advisable for the capacitance value of the input V_{IN} to ground for each channel to be less than 20μF, nor should the output capacitor's capacitance value fall below 200μF. Values lower than these thresholds may compromise the stability of the module's operation. In addition to configuring large-capacity capacitors, multiple smaller capacitors with values such as 1μF and 0.1μF can be externally connected to effectively filter out high-frequency noise.

To suppress surge currents during the startup phase, it is recommended not to leave the TRACK/SS pin floating. A 10nF capacitor should be configured at this pin. Additionally, the resistance value of the PGOOD pull-up resistor is preferably set to 51kΩ.

The capacitance between V_{OUT} and FB serves as the feedforward capacitance. Connecting this capacitor can enhance the phase margin of the system loop within a certain range, thereby improving stability. Reserving the position for this capacitor allows for greater flexibility during system debugging. It is therefore recommended to include this component. Typically, the capacitance value can range from 22pF to 100pF, with a standard value of 22pF.

Product Size



LGA Package

BGA Package

Figure 22. Dimensions of the Shape Unit: mm

Dimension Symbol	Value		
	Min	Nominal	Max
A	4.22	4.32	4.52
A1	4.82	4.92	5.12
D	14.8	15.00	15.20
E	8.80	15.00	15.20
Φb	0.55	0.65	0.73
Φb1	0.66	0.76	0.86
e	—	1.27	—
Z	—	0.52	—

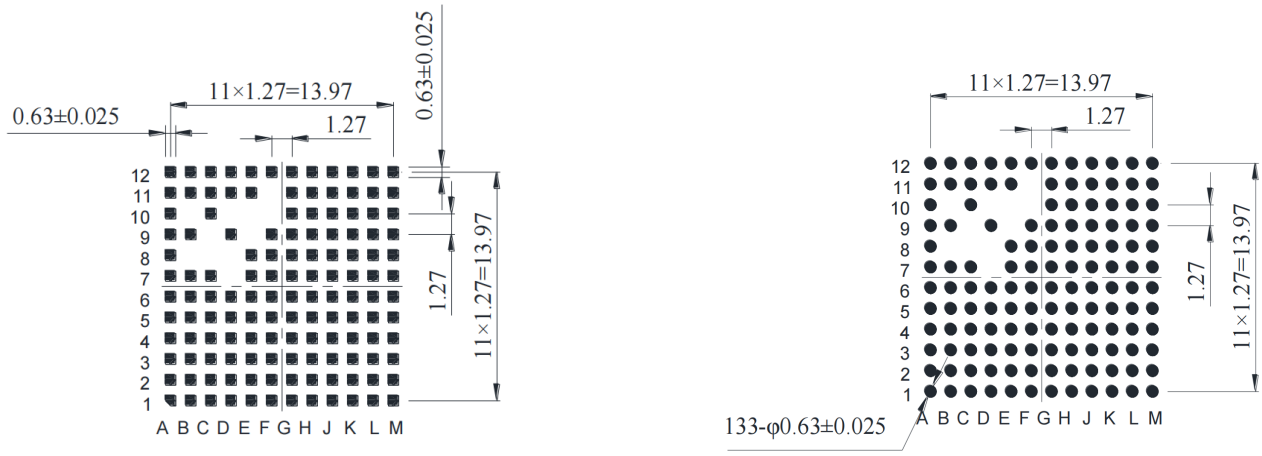


Figure 23. Recommended Pad Size Chart for PCB

Electronics Assembly Instructions

Storage Requirements

For long-term storage, seal the product in an anti-static bag with desiccant under vacuum and store it in an electronic dry cabinet.

If stored post-unsealing under conditions of 30°C and 60% relative humidity (RH), the maximum allowable duration is 168 hours. Products exceeding this period must be baked according to the procedures outlined in IPC/JEDECJ-STD-033 before use or storage. After baking, it is recommended to complete assembly processes (e.g., reflow soldering) within 48 hours. For devices without specified requirements, store in a nitrogen dry cabinet.

Recommended Environmental Process Conditions

1. Product Pre-Treatment

For plastic-encapsulated modules: pre-bake at 125° C for 48 hours before use, or follow IPC/JEDECJ-STD-033B *"Handling, Packaging, Shipping, and Use of Moisture/Reflow-Sensitive Components"* to ensure moisture removal. Complete reflow soldering within 48 hours after baking.

2. Soldering Materials

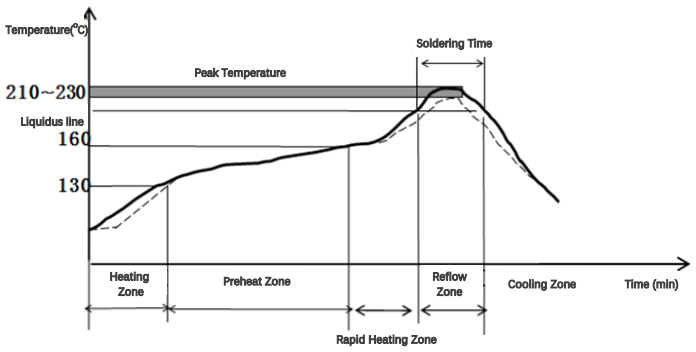
For lead-based soldering, it is recommended to use lead-based solder paste compositions such as Sn63Pb37 or Sn62Pb36Ag2. For lead-free soldering , the use of lead-free solder paste, specifically Sn96. 5Ag3Cu0.5, is advised. The solder paste should comply with a grade of 3 or higher.

3. Component Placement

Align the module's pad centers precisely with the corresponding PCB pads. The solder balls/pads should be pressed into the solder paste to a depth of approximately 0.05mm. Adjust placement pressure to ensure proper contact between pads and solder paste without squeezing paste beyond the pad boundaries. Solder voiding must not exceed 25%.

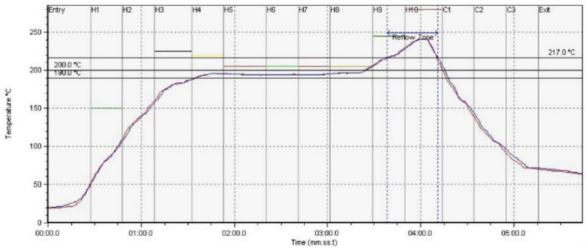
4. Recommended Reflow Profiles

The module is compatible with both lead-based (see Figure 24) and lead-free (see Figure 25) reflow profiles . Use a 9-zone or higher reflow oven to ensure uniform temperature distribution(Note4)



No.	Item	Condition
1	Maximum temperature rise slope in preheat zone	≤3°C/s
2	Maximum temperature drop slope in preheat zone	≤4°C/s
3	Preheat zone duration (130~160°C)	60s~120s
4	Peak temperature in reflow zone	210°C~230°C
5	Reflow zone duration (time ≥183°C for Sn63Pb37)	30S-90S

Figure 24. Typical lead-based reflow soldering profile and parameters.



No.	Item	Condition
1	Heating rate	≤3°C/s
2	Soak zone temperature range	≤4°C/s
3	Soak time	60s~120s
4	Peak temperature	240°C~245°C
5	Time above liquidus (>217°C)	30s~90s
6	Cooling rate	<5°C/s

Figure 25 Typical lead-free reflow soldering profile and parameters.

Note 4: During soldering, the parameters above may be optimized based on the actual component layout. However, the peak temperature must not exceed 245°C. If thick or large metal components require temperatures exceeding 245 °C, thermal shielding measures must be applied to the power module to ensure the actual soldering temperature does not exceed 245°C.

5. Cleaning Clean

using a water-based cleaning agent, followed by drying. Users may adjust the soldering and cleaning processes based on actual conditions, but ultrasonic cleaning is not recommended.

6. Inspection

Inspect the appearance under a microscope to ensure compliance with requirements.

7. X-ray Imaging

Perform X-ray inspection to check solder joint positions, verify solder void compliance, and detect any short circuits. After confirming compliance of the first 1-3 samples, proceed with batch reflow soldering.

Trouble shooting

If a suspected malfunction is observed after device assembly, perform the following checks:
Open Circuit: Inspect solder joints for cold solder joints, insufficient pin soldering, or poor soldering.
No Output: Check the output capacitors near the module.
Short Circuit: Use X-RAY to inspect for internal or external short circuits.

Removal Process

Prior to detaching the module from the PCB, the board must be baked at 125°C for 48 hours to prevent module damage. Skipping this process risks delamination between the epoxy-molded module body and substrate. In severe cases, internal solder may melt and migrate through delamination gaps, causing permanent failure.
It is recommended to utilize a BGA rework station for module removal. The use of a handheld hot air gun is not advised due to the potential for temperatures exceeding 245°C. Furthermore, the product is permitted only one rework cycle.

Precautions

The device must be handled with anti-static measures. Wear anti-static gloves when handling the module to prevent electrostatic discharge (ESD) damage caused by human body charges.
Recommended Operational Practices:
a) Operate the device on an anti-static workbench or use finger cots.
b) Ensure all testing equipment and tools are properly grounded.
c) Avoid touching the device leads directly.d) Store the device in anti-static containers (e.g., ESD-safe boxes).
e) During production, testing, usage, and transportation, avoid materials that generate static electricity (e.g., plastics, rubber, silk fabrics).
f) Maintain relative humidity between 30%~70%.