# MCCPA1013-P37

**1060-1380MHz CW 37dBm Power Amplifier**

## Product Overview

MCCPA1013-P37 is a two-stage HBT small cell power amp -lifier for indoor cellular base stations.It works at 1060-1380MHz.This PA can deliver CW 37dBm output power with 28dB gain.

ROHS compliant

Evaluation boards are available upon request.


14 Pin 7×7mm Laminate Package

*Figure1.*

## Functional Block Diagram

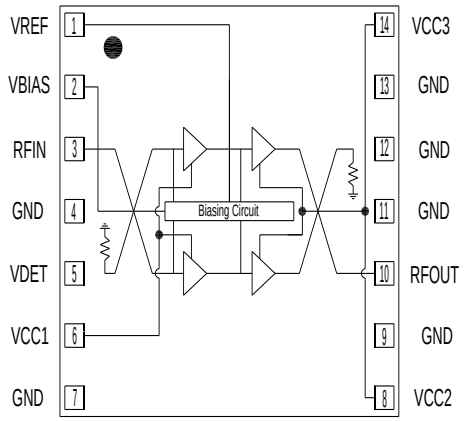



*Figure2.*

## Key Features

- Frequency Range: 1060-1380MHz
- 28dB Gain @36dBm
- 40% PAE at 37dBm output power
- 37dBm CW peak output power
- Input/output internally matched to 50Ω
- Integrated temperature compensation circuits
- Compact and low-cost 5mm×5mm LGA package (MSL3,260℃ per JEDEC J-STD-020)

## Applications

- FDD and TDD 2G/3G/4G LTE/5G NR systems
- Driver amplifier for micro-base and macro-base stations
- Active antenna array and massive MIMO
- Customer Premises Equipment(CPE)

## Ordering info

| Part No. | Description |
|---|---|
| MCCPA1013-P37 | 7' Reel with 1500pcs |

## Pin Description

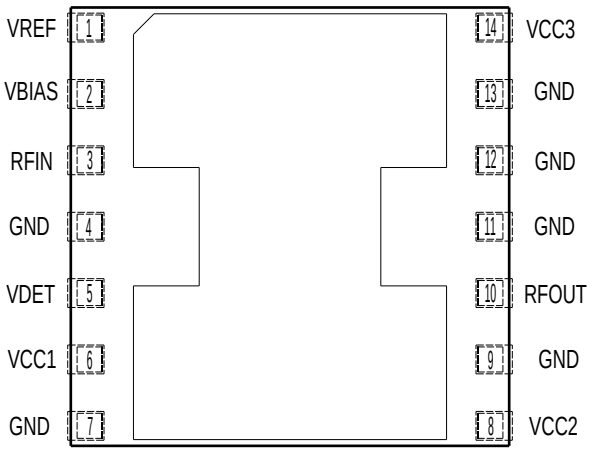



*Figure 3.Pinout (Top View)*

| Pin | Name | Description | Pin | Name | Description |
|---|---|---|---|---|---|
| 1 | VREF | Reference Voltage | 8 | VCC2 | Stage 2 collector voltage |
| 2 | VBIAS | Bias Voltage | 9 | GND | Ground |
| 3 | RFIN | RF input port | 10 | RFOUT | RF output port |
| 4 | GND | Ground | 11 | GND | Ground |
| 5 | VDET | Power detector DC output | 12 | GND | Ground |
| 6 | VCC1 | Stage 1 collector voltage | 13 | GND | Ground |
| 7 | GND | Ground | 14 | VCC3 | Stage 3 collector voltage |

## Absolute Maximum Ratings[1]

| Parameter | Rating | Unit |
|---|---|---|
| Operating Temp,$T_C$ | -40 to +85 | °C |
| Operating Junction Temp,$T_J$ | 175 | °C |
| Storage Temp,$T_{STG}$ | -55 to+125 | °C |
| Thermal Resistance,$R_{\theta jc}$ | 10.2 | °C/W |
| Operating Voltage,$V_{CC1}$,$V_{CC2}$,$V_{CC3}$,$V_{BIAS}$ | 5.5 | V |
| Inuput Power,$P_{IN}$ | 20 | dBm |

Notes[1]: Exceeding any one or a combination of the Absolute Maxium Rating conditions may cause permanent damage to the device. Extended application of the Absolute Maximum Rating conditions to the device mayreduce device reliability.

## Recommended Operating Conditions

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Operating Frequency,F | 1060 | | 1380 | MHz |
| Operating Temp,TC | -40 | 25 | 85 | ℃ |
| Operating Voltage, $V_{CC1}$,$V_{CC2}$,$V_{CC3}$,$V_{BIAS}$ | 4.5 | 5 | 5.5 | V |
| Reference Voltage,$V_{REF}$ | 2.8 | 2.95 | 3.05 | V |
| Reference Current,$I_{REF}$ | | 20 | 30 | mA |

## Electrical Specifications-EVB Typical Performance[1]

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Frequency | | 1060 | | 1380 | MHz |
| Peak Output Power | CW | | 37 | | dBm |
| Gain @36dBm | | | 28 | | dB |
| Power added efficiency | CW,37dBm | | | 40 | % |
| Quiescent current | | | 600 | | mA |
| ACPR@＋28dBm | 20MHz LTE-TM3.1,9.5dB PAR | | / | | dBc |
| Instantaneous bandwidth | | | 60 | | MHz |
| Iutput/Output Impendance | | | 50 | | Ω |

Notes[1]:$V_{CC1}$=$V_{CC2}$=$V_{CC3}$=$V_{BIAS}$=5V,$V_{REF}$=2.95V,F=1240MHz,Signal=CW,TC=25℃,Input/Output Load=50Ω

## Detector Specifications[1]

| Output Power(dBm) | $V_{DET}$(mV) | Output Power(dBm) | $V_{DET}$(mV) |
|---|---|---|---|
| 29 | 886 | 23 | 525 |
| 28 | 809 | 22 | 487 |
| 27 | 737 | 21 | 435 |
| 26 | 673 | 20 | 422 |
| 25 | 615 | | |
| 24 | 568 | | |

Notes[1]:VCC1=VCC2=VCC3=VBIAS=5V,VREF=2.95V,F=1240MHz,Signal=CW,TC=25℃,Input/Output Load=50Ω.

## Evaluation Board Schemic

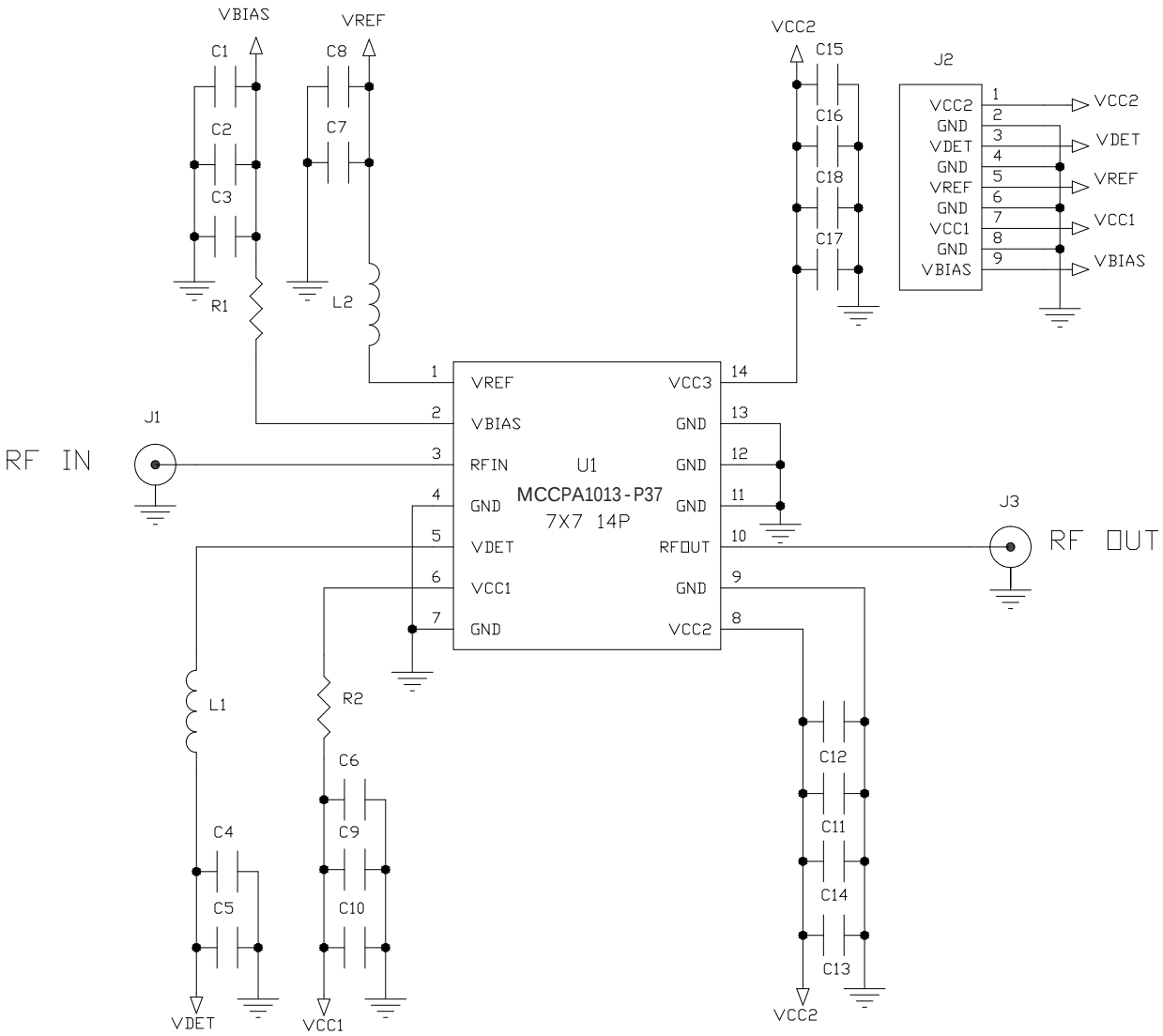



*Figure 4. Evaluation Board Schemic*

## Evaluation Board Bill of Materials

| Ref,Des | Value | Size |
|---|---|---|
| C1 C14 C15 C8 C10 | Ceramic capacitor, 4.7uF, 16V, +/-10%, X7R | 1206 |
| L1 L2 R1 R2 | Resistor, 0 Ω, 0.063W | 0402 |
| C4 | Ceramic capacitor, 2.2nF, 16V, +/-10%, X7R | 0402 |
| C19 | Ceramic capacitor, /pF, 16V, +/-10%, X7R | 0402 |

Rest of the components on the schematic are not used in this part.

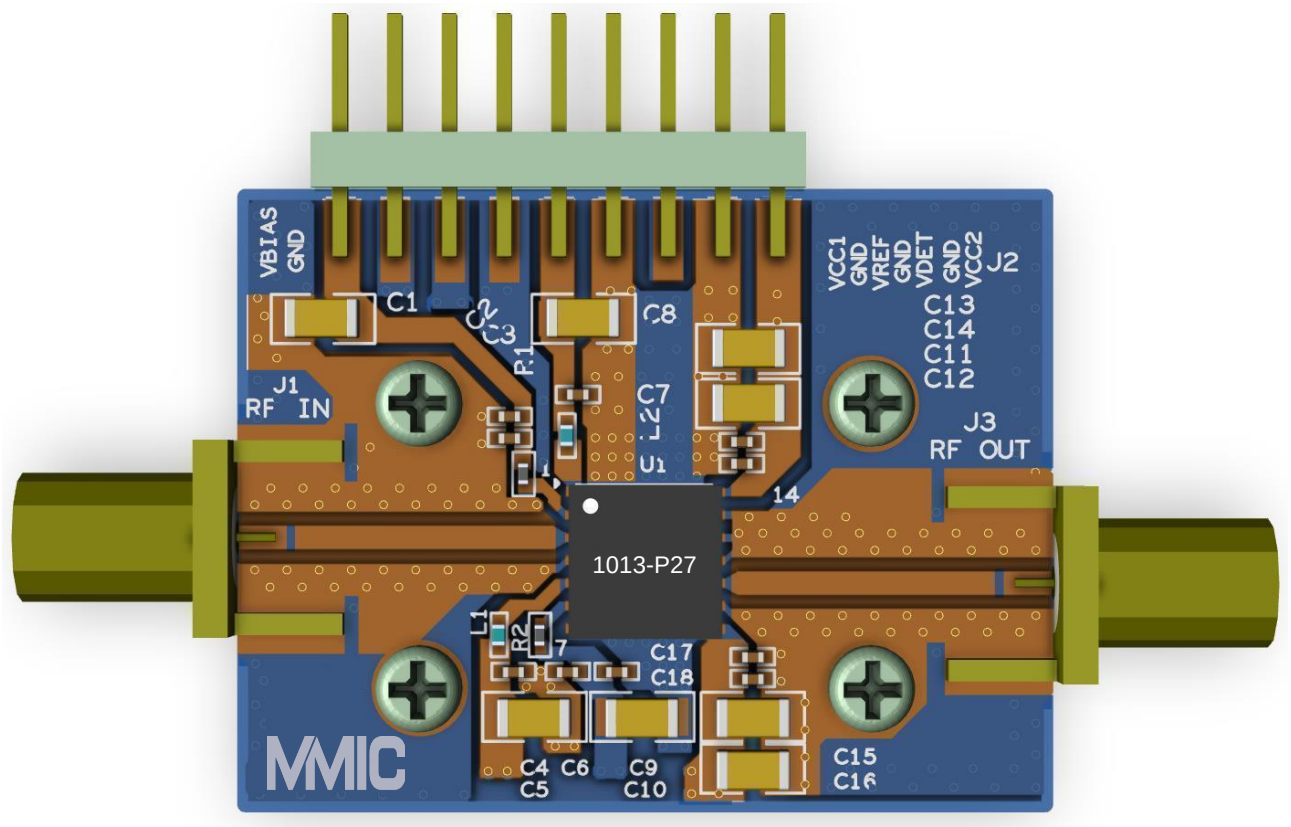



*Figure 5 .Evaluation Board PCB information*

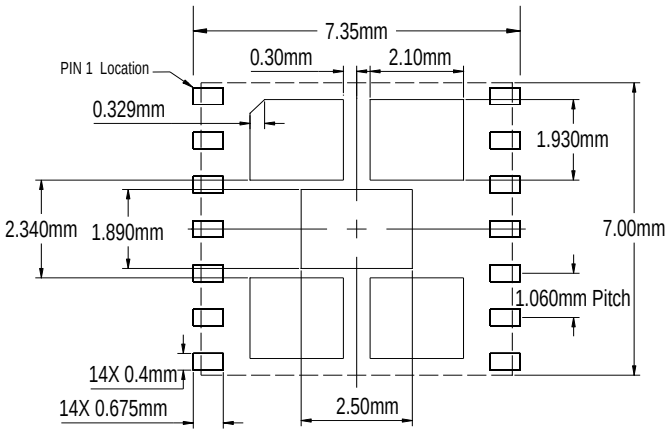
## Evaluation board test procedure

### Turn-on sequence

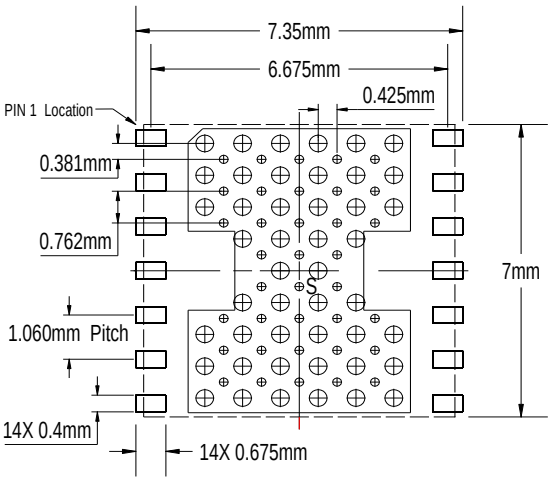
1.Connect test equipment to the input and output port of Evaluation board and then connect DC ground.
2.Turn on VCC1,VCC2,VCC3 to 5V, turn on VBIAS to 5V then turn on VREF to 2.95V in order.
3.Apply RF signal

### Turn-on sequence

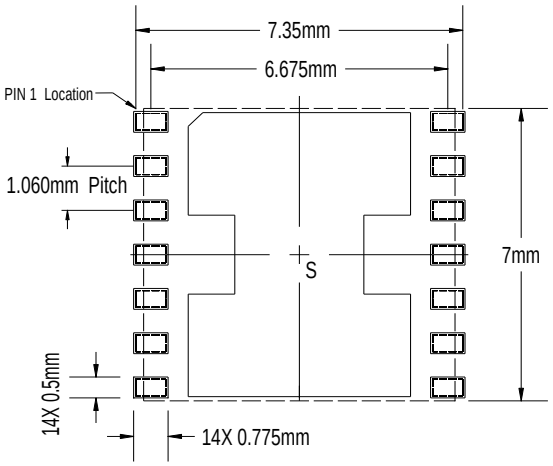
1.Turn off RF signal
2.Turn off VREF,VBIAS,VCC1,VCC2 ,VCC3 in order




Stencil Aperture Top View




Metallization Top View




Solder Mask Opening Top View

Notes:
*(1) UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.*
*(2) VIAS SHOWN IN PCB METAL VIEW ARE FOR REFERENCE ONLY.*
*NUMBER & SIZE OF THERMEL VIAS REQUIRED DEPENDENT ON HEAT DISSIPATION REQUIREMENT AND THE PCB PROCESS CAPABILITY.*

DETAIL S
SHAPE
1X THIS ROTATION

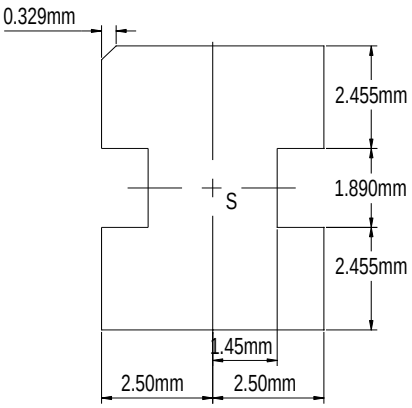
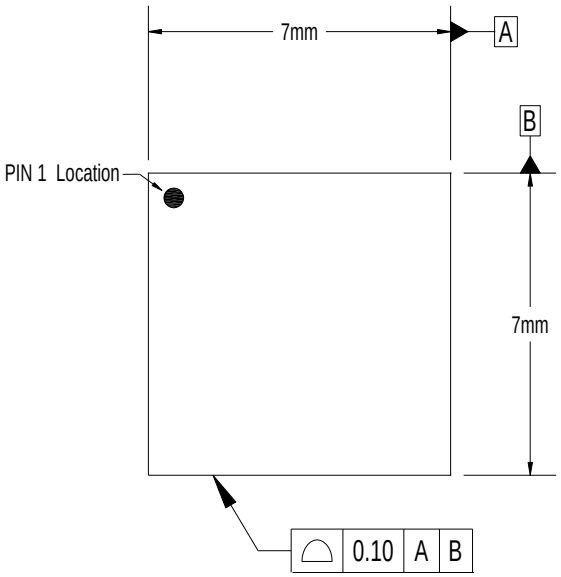
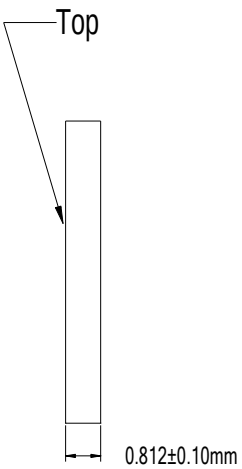



*Figure 6.PCB Layout Footprint*

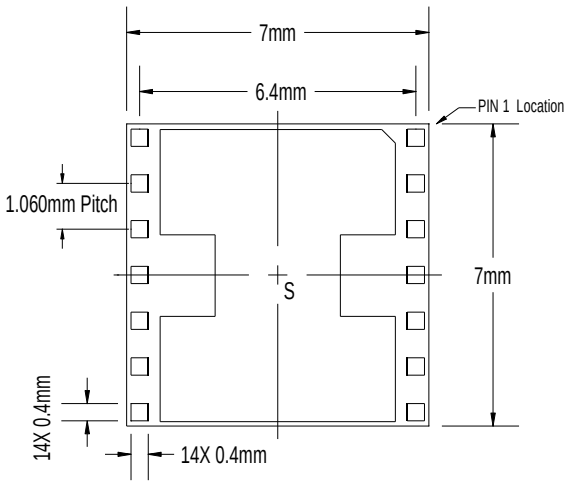
## Package Dimensions




Top View




SIDE VIEW




BOTTOM VIEW

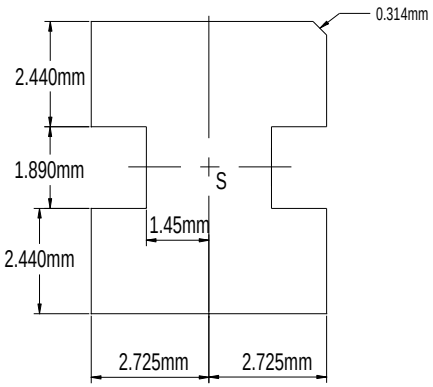



*Figure 7.Package Dimensions*

*Notes:*

*1.Tolerance is ±0.050mm unless otherwise specified.*

*2.Among the 14pins on both sides, the size of the GND pin is 0.06mm larger than that of the other pins*

## Tape and Reel Information

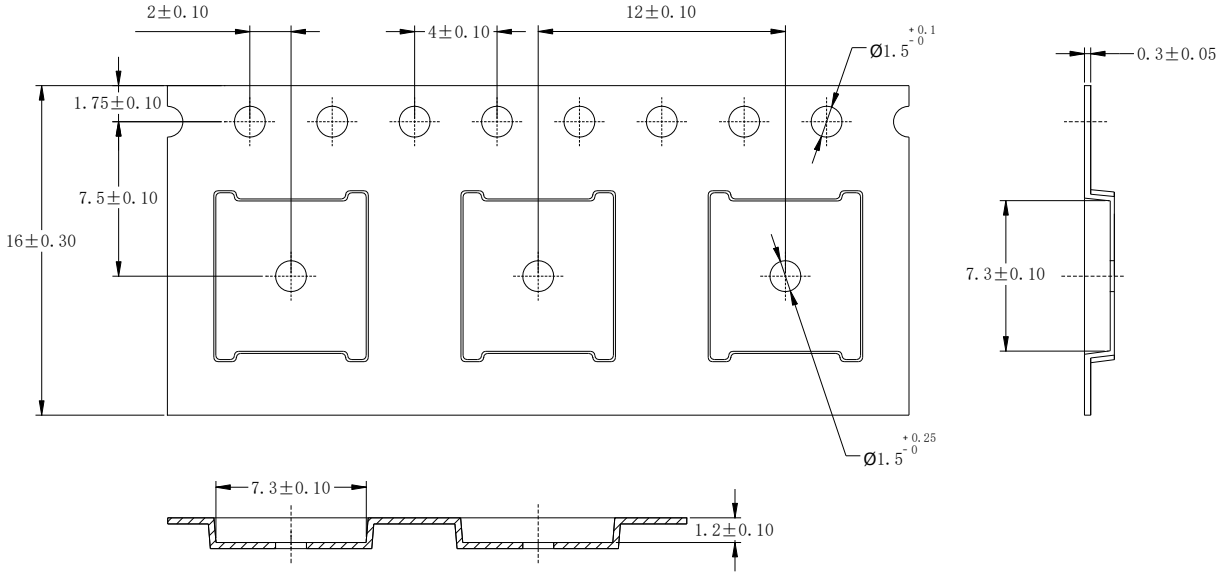



*Figure 8*

*Technical requirements:*
*1. The Material :PS*
*2.MOLD# LGA/QFN(7×7)*
*3.Cover Tape Width: 13.3±0.1mm*
*4.Cover Tape Color:Transparent*
*5.Carrier tape color:Black.*