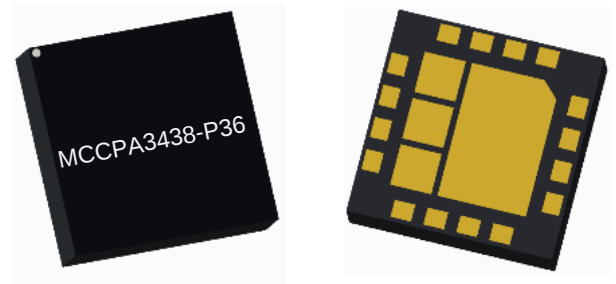


Product Overview

The MCCPA3438-P36 is a three-stage HBT general purpose power amplifier working at 3400~3800 MHz(Band 42,n78) with on-chip PA enable controller and temperature compensation circuits. This high-efficiency and DPD-friendly PA can deliver up to 28dBm average output power and 38dBm peak power using 20MHz LTE signal(9.5dB PAR@0.01%CCDF). The product input and output are both internally matched to 50Ω.

ROHS compliant

Evaluation boards are available upon request.



16Pad 5×5mm Laminate Package

Figure1.

Functional Block Diagram

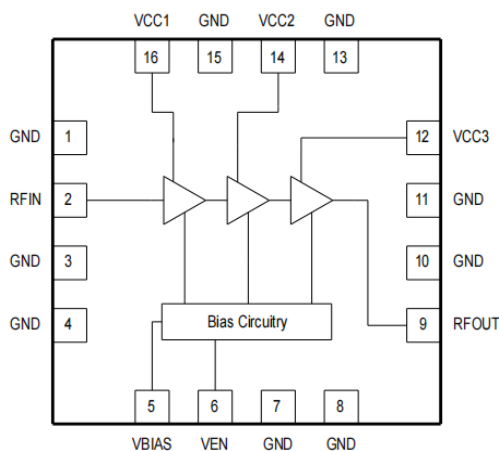


Figure2.

Key Features

- Frequency Range: 3400-3800MHz
- 30dB Gain
- 23% PAE at 28dBm output power
- Below -33dBc ACPR at 28dBm output power
- Higher than 38dBm peak power
- Wide instantaneous BW DPD friendly design
- Input/Output internally matched to 50Ω
- On-chip PA enable controller and temperature compensation circuits
- Compact and low-cost 5mm×5mm LGA package (MSL3,260 per JEDEC J-STD-020)

Applications

- FDD and TDD 2G/3G/4G LTE/5G NR systems
- 3GPP band 42,5G n78 small-cell base stations
- Customer Premises Equipment (CPE)
- Active antenna array and massive MIMO
- Driver amplifier for micro-base and macro-base stations

Ordering info

Part No.	Description
MCCPA3438-P36	7' Reel with 1500pcs

Pin Description

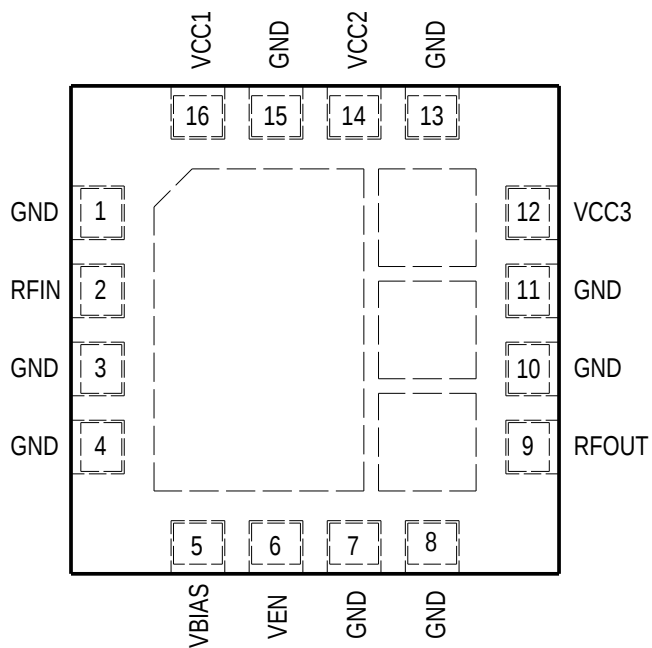


Figure 3. Pinout (Top View)

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	9	RFOUT	RF output port
2	RFIN	RF input port	10	GND	Ground
3	GND	Ground	11	GND	Ground
4	GND	Ground	12	VCC3	Stage 3 collector voltage
5	VBIAS	Bias voltage	13	GND	Ground
6	VEN	PA enable voltage	14	VCC2	Stage 2 collector voltage
7	GND	Ground	15	GND	Ground
8	GND	Ground	16	VCC1	Stage 1 collector voltage

Absolute Maximum Ratings¹

Parameter	Rating	Unit
Operating Temp,Tc	-40 to +105	
Operating Junction Temp,Tj	150	
Storage Temp,TSTG	-55 to+125	
Thermal Resistance,Rθjc	21.1	/W
Operating Voltage,VCC1,VCC2,VCC3,VBIAS	5.5	V
Inuput Power,PIN	10	dBm

Notes¹: Exceeding any one or a combination of the Absolute Maxium Rating conditions may cause permanent damage to the device. Extended application of the Absolute Maximum Rating conditions to the device mayreduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Frequency,F	3400		3800	MHz
Operating Temp,Tc	-40	25	85	
Operating Voltage,Vcc1,Vcc2,Vcc3	4.5	5	5.5	V
PA Enable Voltage,VEN	1.6	1.8	3	V
PA Enable Current,IEN		400		uA

Electrical Specifications¹

Parameter	Conditions	Min	Typ	Max	Unit
Frequency		3400		3800	MHz
Tested Frequency			3600		MHz
Output average power			+28		dBm
Output P3dB	Pulse 10%,1ms		+37		dBm
Gain @28dBm	Pulse 10%,1ms	27	31		dB
Power added efficiency	Pulse 10%,1ms		23		%
ACPR@28dBm	20MHz LTE E-TM1.1,9.5dB PAR		-33		dBc
Quiescent current	RF OFF	90	150		mA
Iutput return loss			-10		dB
Reverse isolation			-51		dB
Instantaneous bandwidth			200		MHZ

Notes¹:VCC1=VCC2=VCC3=VBIAS=5V, VEN=1.8V,F=3700MHz,TC=25 Input/Output Load=50Ω

Evaluation Board Schemic

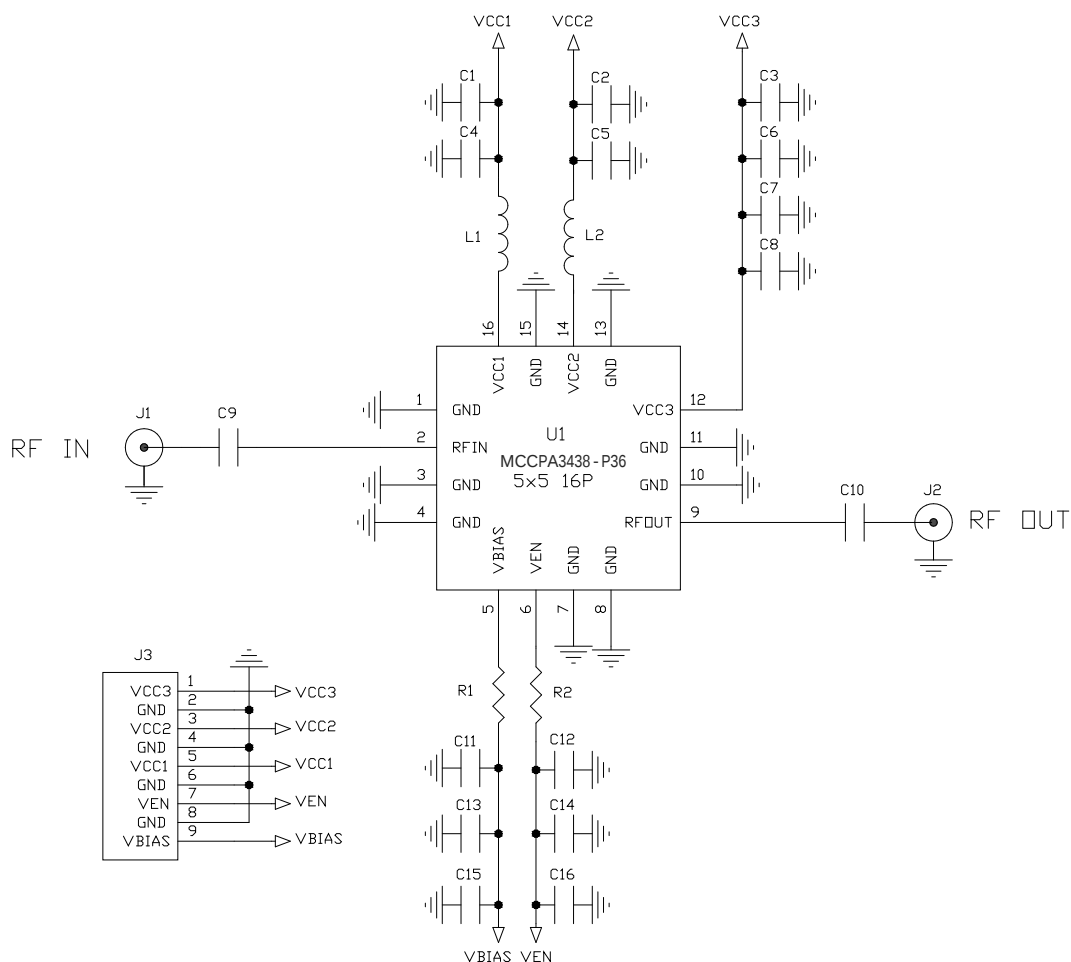


Figure 4. Evaluation Board Schemic

Evaluation Board Bill of Materials

Ref,Des	Value	Size
C9 C10	Ceramic capacitor, 18pF, 16V, +/-10%, X7R	0402/0603
C1 C2 C6 C15	Ceramic capacitor, 4.7uF, 16V, +/-10%, X7R	1206
L1 L2 R1 R2	Resistor, 0 Ω , 0.063W	0402
C12	Ceramic capacitor, 2.2nF, 16V, +/-10%, X7R	0402

Rest of Components on the schematic are not used in this part.

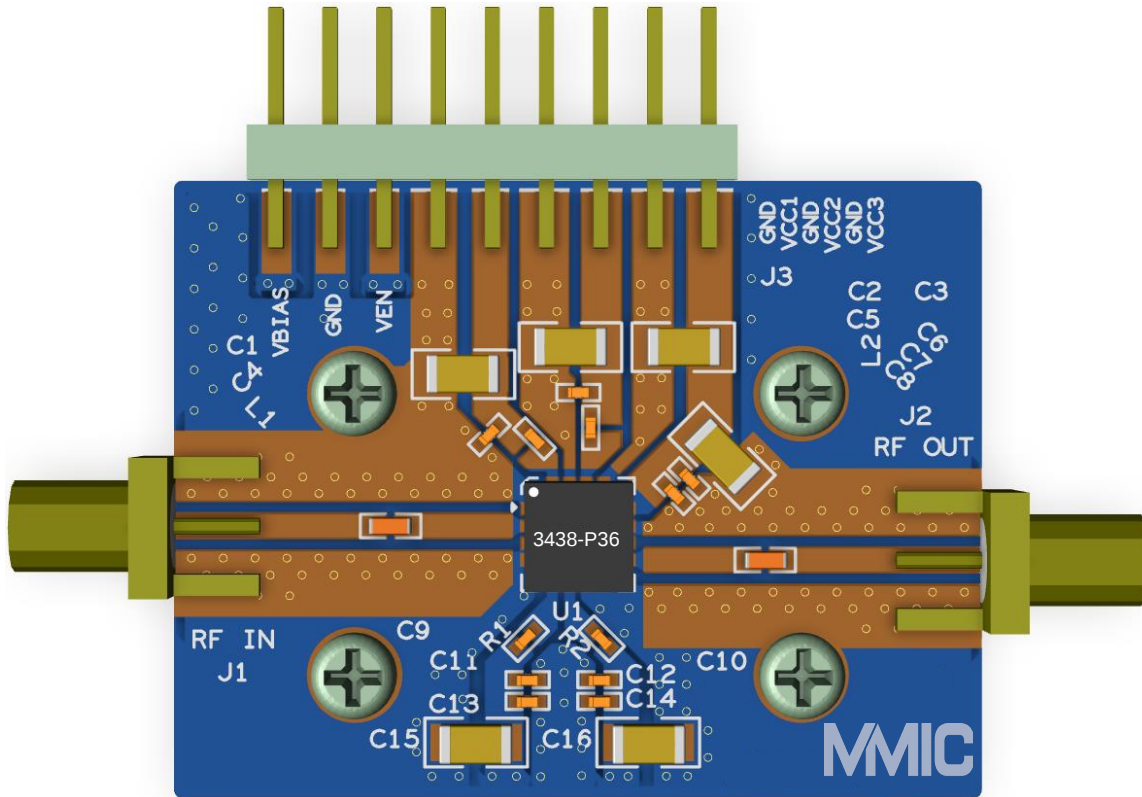


Figure 5 .Evaluation Board PCB information

Evaluation board test procedure

Turn-on sequence

- 1.Connect test equipment to the input and output port of Evaluation board and then connect DC ground.
- 2.Turn on VCC1,VCC2,VCC3 to 5V,turn on VBIAS to 5V then turn on VEN to 1.8V in order.
- 3.Apply RF signal

Turn-on sequence

- 1.Turn off RF signal
- 2.Turn off VEN,VCC1,VCC2 and VCC3 in order

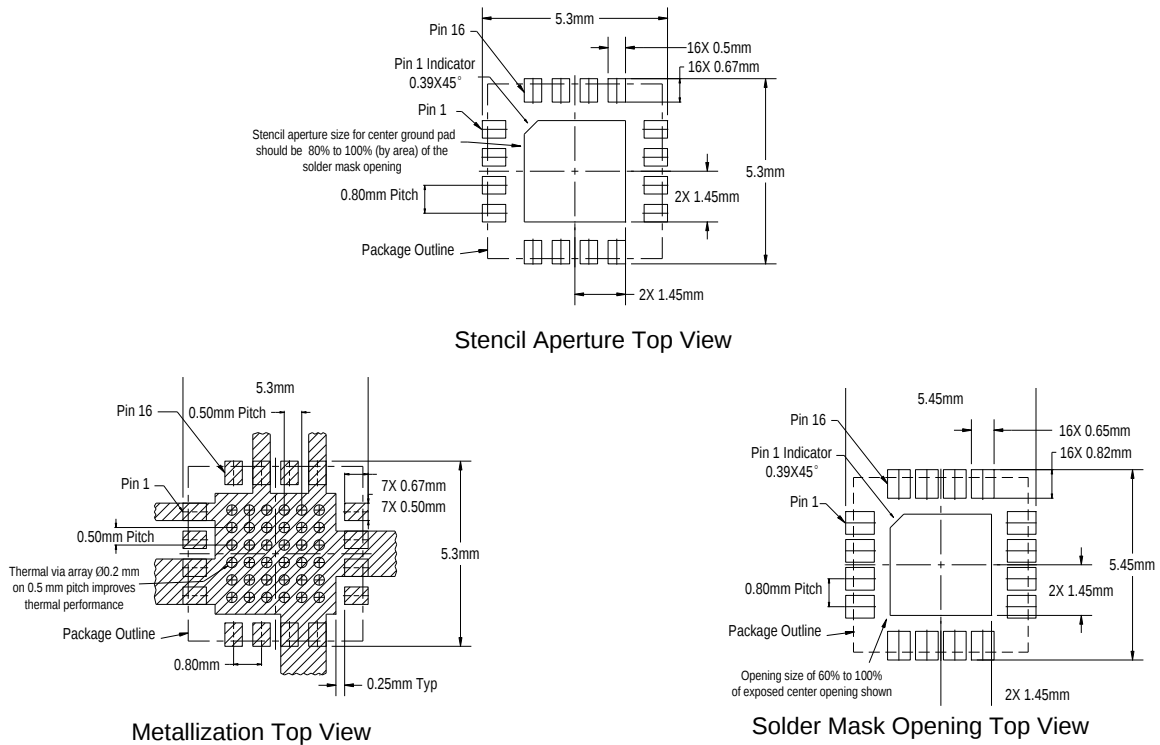


Figure 6. PCB Layout Footprint

Package Dimensions

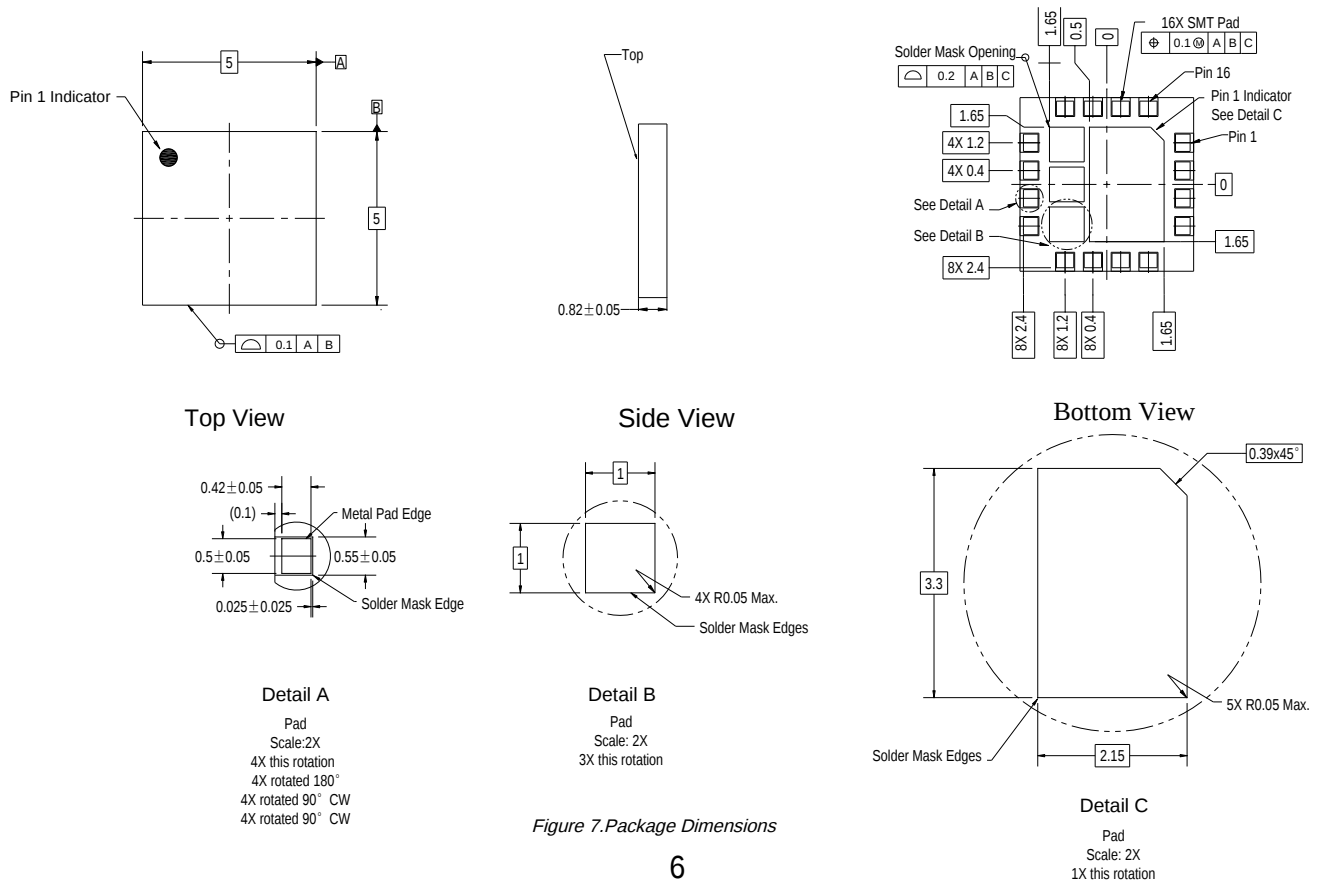


Figure 7. Package Dimensions

Technical drawing of a mechanical part, showing a top view and a side view. The part is rectangular with rounded ends and features a central horizontal slot. Dimensions are given in millimeters (mm).

Top View Dimensions:

- Overall width: 12 ± 0.30
- Overall length: 5.3 ± 0.10
- Distance from left edge to first hole center: 0.3 ± 0.05
- Distance between hole centers: 2 ± 0.10
- Distance from last hole center to right edge: 4 ± 0.10
- Distance from left edge to first square feature: 1.1 ± 0.10
- Distance between square feature centers: 8 ± 0.10
- Distance from last square feature center to right edge: 1.75 ± 0.10
- Distance from top edge to hole center: 5.5 ± 0.10

Top View Callouts:

- $\varnothing 1.5^{+0.1}_{-0}$ (Hole diameter)
- PIN 1 (Pin location)
- $\varnothing 1.5^{+0.25}_{-0}$ (Hole diameter)

Side View Dimensions:

- Overall height: 5.3 ± 0.10
- Distance from bottom edge to top edge of slot: 4°

Side View Callouts:

- $\varnothing 1.5^{+0.1}_{-0}$ (Hole diameter)

1. Cover tape color: Black
2. The material: PS
3. Mold# LGA/QFN(5×5)
4. Cover tape width: $9.5 \pm 0.1 \text{ mm}$ / $9.3 \pm 0.1 \text{ mm}$
5. Cover tape color: transparent

Figure 8